

Compal Confidential

JDC40 MB Schematic Document

LA-N411P

Rev: 1.0 (A00)

2023.12.25

Oasis MTL 14"16" UMA(LPDDR5x)

Meteor Lake U

Layout Dell logo

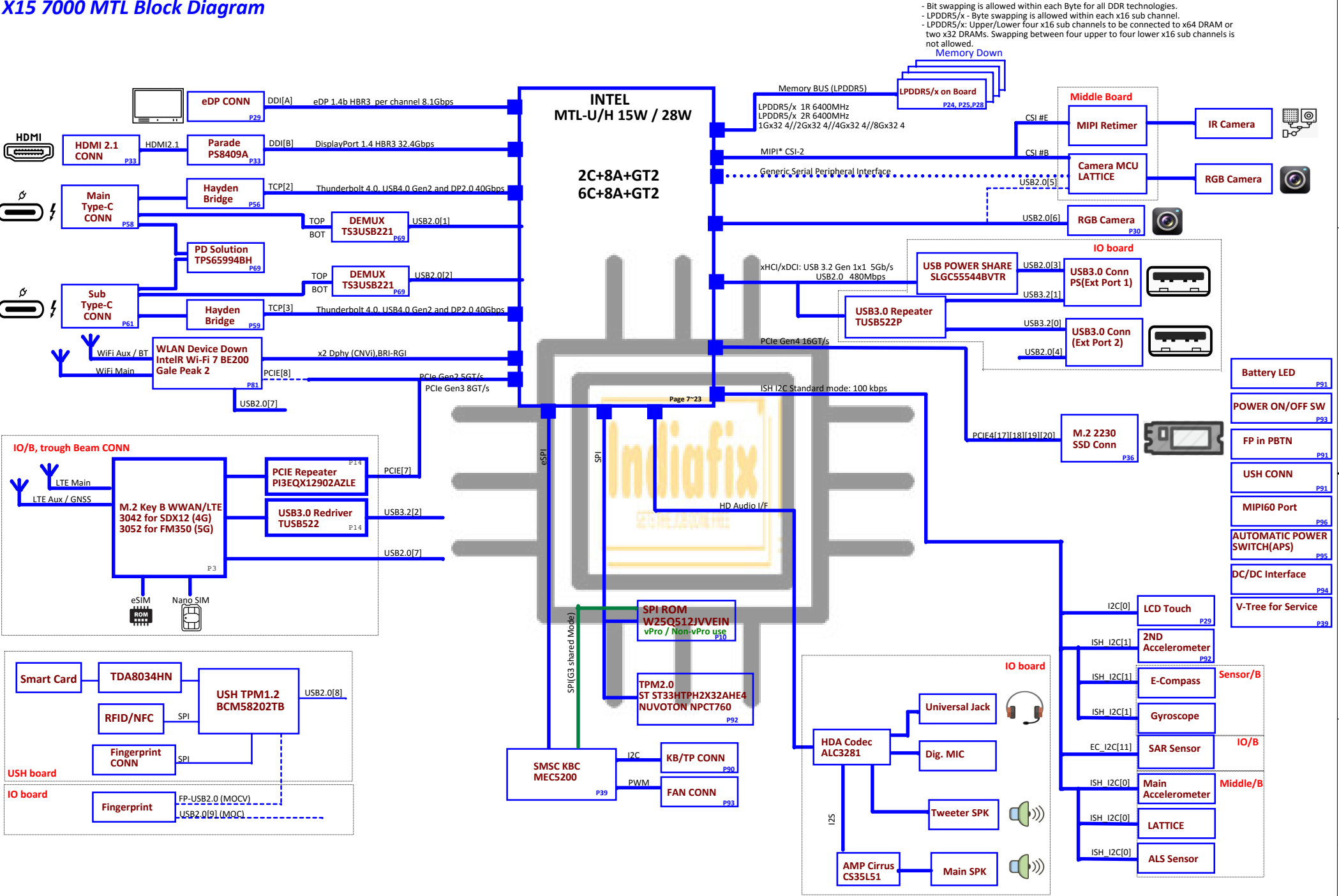


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X15 7000 MTL Block Diagram



- Bit swapping is allowed within each Byte for all DDR technologies.
- LPDDR5/x - Byte swapping is allowed within each x16 sub channel.
- LPDDR5/x: Upper/Lower four x16 sub channels to be connected to x64 DRAM or two x32 DRAMs. Swapping between four upper to four lower x16 sub channels is not allowed.

Figure 32. MTL-H Supported PCI Express* Link Configurations

MTL-H	SoC (System On Chip) Tile												IOE (IO Expander) Tile															
	FIA-2								FIA-3				FIA-4				FIA-5											
Flex I/O Lanes	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29
PCIe Controller	1				2				3				4				5				6							
PCIe Max Rate	Gen4				Gen4				Gen4				Gen4				Gen4				Gen5							
PCIe Lanes	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28
PCIe Configurations (Bi-Furcation) ³	1px4				1px4				1px4				1px4				1px4				1px8							
	1px4(LR)				1px4(LR)				1px4(LR)				1px4(LR)				1px4(LR)				1px8(LR)							
	2px2				2px2																							
	2px2(LR)				2px2(LR)																							
	1px2+2px1				1px2+2px1																							
Logical Link Lanes	2px1+1px2 ²				2px1+1px2 ²																							
	4px1				4px1																							
	0	1	2	3	0	1	2	3	0	1	2	3	0	1	2	3	0	1	2	3	0	1	2	3	4	5	6	7
	3	2	1	0	3	2	1	0	3	2	1	0	3	2	1	0	3	2	1	0	7	6	5	4	3	2	1	0
	0	1	0	1	0	1	0	1	0																			
Assigned Root Ports	RP1				RP5				RP9				RP10				RP11				RP12							
	RP1				RP5				RP9				RP10				RP11				RP12							
	RP1				RP5				RP9				RP10				RP11				RP12							
	RP1				RP5				RP9				RP10				RP11				RP12							
	RP1				RP5				RP9				RP10				RP11				RP12							
Bus - Dev - Func (BDF) Assignments ¹	RP	Bus	Dev	Func	RP	Bus	Dev	Func	RP	Bus	Dev	Func	RP	Bus	Dev	Func	RP	Bus	Dev	Func	RP	Bus	Dev	Func	RP	Bus	Dev	Func
	1	0h	1Ch	0h	5	0h	1Ch	4h	9	0h	6h	0h	10	0h	6h	1h	11	0h	6h	2h	12	0h	1h	0h				
	2	0h	1Ch	1h	6	0h	1Ch	5h																				
	3	0h	1Ch	2h	7	0h	1Ch	6h																				
	4	0h	1Ch	3h	8	0h	1Ch	7h																				

U15 NC

U15 NC

MTL P Flexible HSIO Lane Details

Flex-IO Lane	USB3.2	GbE	PCIE	SATA	DEVICE
FIL [0]	USB3-1				Type-A Port 1
FIL [1]	USB3-2				Type-A Port 2
FIL [2]			PCIE-1	SATA 0	
FIL [3]			PCIE-2	SATA 1	
FIL [4]			PCIE-3		
FIL [5]			PCIE-4		
FIL [6]			PCIE-5		
FIL [7]			PCIE-6		
FIL [8]			PCIE-7		M.2 3042(WWAN)
FIL [9]			PCIE-8		M.2 2230(WLAN)
FIL [10]			PCIE-9		
FIL [11]			PCIE-10		
FIL [12]			PCIE-11		
FIL [13]			PCIE-12		
FIL [14]			PCIE-13		
FIL [15]			PCIE-14		
FIL [16]			PCIE-15		
FIL [17]			PCIE-16		
FIL [18]			PCIE-17		M.2 2230 SSD
FIL [19]			PCIE-18		M.2 2230 SSD
FIL [20]			PCIE-19		M.2 2230 SSD
FIL [21]			PCIE-20		M.2 2230 SSD

*A maximum of 9 PCIe Root Ports (or devices) can be enabled when GbE Port is disabled
*A maximum of 8 PCIe Root Ports (or devices) can be enabled when GbE Port is enabled

PCH USB2.0	DEVICE
1	Type-C Port 1(Rear)
2	Type-C Port 2(Front)
3	Ext USB Port 1 Charge
4	Ext USB Port 2
5	Middle/B MCU
6	Camera
7	M.2 3042(WWAN)
8	USH
9	Finger Print MOC
10	M.2 2230(BT)

CPU HS PORT	DEVICE
DDI-A	EDP
DDI-B	HDMI
TCP0	USB3 port2
TCP1	NA
TCP2	Type-C Port1
TCP3	Type-C Port2

BOM Structure Table

Function	Stuff	Un-Stuff
Nopop Component		@
Connector Component	CONN@	
Jump solder and short	JUMP@	@JUMP@
EMI Component	EMI@	@EMI@
ESD Component	ESD@	@ESD@
RF Component	RF@	@RF@
WWAN Component	WWAN@	@WWAN@
Non WWAN Component	NWWAN@	
TPM Component	ST33@	
	NU@	@NU@
vPro Component	VPRO@	
Non-vPro Component	NVPRO@	
Re-Timer BB Component	BB@	
Re-Timer HBR Component	HBR@	
USB2 MUX Component	U2MUX@	
Non USB2 MUX Component	NU2MUX@	
MEC5107 Component	5107@	
MEC5200 Component	5200@	
MIPI Component	MIPI60@	
Non MIPI Pop Component	NMIP60@	
DUDC Component	DUDC@	
Non DUDC Pop Component	NDUDC@	
CCD Component	CCD@	

Voltage Rails

Refer to PDG "power states" section									
Rails	Rail (Project Net)	S0/M0	C10	S0ix/Moff	S3/M3	S3/Moff	S4 and S5/M3	S4 and S5/Moff	G3
VCCRTC	+RTC_CELL_PCH_1P5	ON	ON	ON	ON	ON	ON	ON	ON
VBATA(VDC)	+13.5VB	ON	ON	ON	ON	ON	ON	ON	No Power
VCCPRIM_3P3	+3.3V PRIM	ON	ON	ON	ON	ON	ON	ON	No Power
VCCPRIM_1P8	+1.8V PRIM	ON	ON	ON	ON	ON	ON	ON	No Power
VCCPRIM_IO	+VCCPRIM_IO	ON	ON	ON	ON	ON	ON	ON	No Power
VCCPRIM_VNNAON	+VCCPRIM_VNNAON	ON	ON	ON	ON	ON	ON	ON	No Power
V3.3M	subsystem 3.3V	ON	ON	OFF	ON	OFF	ON	OFF	No Power
V1.8M	subsystem 1.8V	ON	ON	OFF	ON	OFF	ON	OFF	No Power
VDD2	+1.065V_MEM	ON	ON	ON	ON	ON	OFF	OFF	No Power
VPP	+1.8V MEM	ON	ON	ON	ON	OFF	OFF	OFF	No Power
VCCSA	+VCCSA	ON	OFF	OFF	OFF	OFF	OFF	OFF	No Power
VCCCORE	+VCCIA	ON	OFF	OFF	OFF	OFF	OFF	OFF	No Power
VCCGT	+VCCGT	ON	OFF	OFF	OFF	OFF	OFF	OFF	No Power

Base line	
Contingency	

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X76 DRAM Option

LPDDR5x	Hynix 16GB			
	UD1 H16GX@ SA0000FW12L	UD2 H16GX@ SA0000FW12L	UD3 H16GX@ SA0000FW12L	UD4 H16GX@ SA0000FW12L
LPDDR5x	Samsung 16GB			
	UD1 S16GX@ SA0000FPJ2L	UD2 S16GX@ SA0000FPJ2L	UD3 S16GX@ SA0000FPJ2L	UD4 S16GX@ SA0000FPJ2L
LPDDR5x	Micron 32GB			
	UD1 M32GX@ SA0000FM11L	UD2 M32GX@ SA0000FM11L	UD3 M32GX@ SA0000FM11L	UD4 M32GX@ SA0000FM11L
LPDDR5x	Micron 64GB			
	UD1 M64GX@ SA0000FM21L	UD2 M64GX@ SA0000FM21L	UD3 M64GX@ SA0000FM21L	UD4 M64GX@ SA0000FM21L
LPDDR5x	Micron 16GB			
	UD1 M16GX@ SA0000FM01L	UD2 M16GX@ SA0000FM01L	UD3 M16GX@ SA0000FM01L	UD4 M16GX@ SA0000FM01L
LPDDR5x	Samsung 64GB			
	UD1 S64GX@ SA0000FPK2L	UD2 S64GX@ SA0000FPK2L	UD3 S64GX@ SA0000FPK2L	UD4 S64GX@ SA0000FPK2L
LPDDR5x	Hynix 64GB			
	UD1 H64GX@ SA0000FW52L	UD2 H64GX@ SA0000FW52L	UD3 H64GX@ SA0000FW52L	UD4 H64GX@ SA0000FW52L
LPDDR5x	Samsung 32GB			
	UD1 S32GX@ SA0000FSQ2L	UD2 S32GX@ SA0000FSQ2L	UD3 S32GX@ SA0000FSQ2L	UD4 S32GX@ SA0000FSQ2L
LPDDR5x	Hynix 32GB			
	UD1 H32GX@ SA0000FW32L	UD2 H32GX@ SA0000FW32L	UD3 H32GX@ SA0000FW32L	UD4 H32GX@ SA0000FW32L

DRAM Config Option
(Resistor pop location)

MEM_CONFIG0		MEM_CONFIG1		MEM_CONFIG2		MEM_CONFIG3		MEM_CONFIG4		MEM_CONFIG5	
RC373 H16GX@ SD043100280	RC374 H16GX@ SD043100280	RC377 H16GX@ SD043100280	RC379 H16GX@ SD043100280	RC380 H16GX@ SD043100280	RC900 H16GX@ SD043100280	RC373 S16GX@ SD043100280	RC375 S16GX@ SD043100280	RC376 S16GX@ SD043100280	RC379 S16GX@ SD043100280	RC380 S16GX@ SD043100280	RC900 S16GX@ SD043100280
RC373 M32GX@ SD043100280	RC375 M32GX@ SD043100280	RC377 M32GX@ SD043100280	RC379 M32GX@ SD043100280	RC381 M32GX@ SD043100280	RC901 M32GX@ SD043100280	RC373 M64GX@ SD043100280	RC375 M64GX@ SD043100280	RC377 M64GX@ SD043100280	RC378 M64GX@ SD043100280	RC380 M64GX@ SD043100280	RC901 M64GX@ SD043100280
RC373 M16GX@ SD043100280	RC375 M16GX@ SD043100280	RC377 M16GX@ SD043100280	RC379 M16GX@ SD043100280	RC380 M16GX@ SD043100280	RC900 M16GX@ SD043100280	RC373 S64GX@ SD043100280	RC375 S64GX@ SD043100280	RC376 S64GX@ SD043100280	RC378 S64GX@ SD043100280	RC380 S64GX@ SD043100280	RC901 S64GX@ SD043100280
RC373 H64GX@ SD043100280	RC374 H64GX@ SD043100280	RC377 H64GX@ SD043100280	RC378 H64GX@ SD043100280	RC380 H64GX@ SD043100280	RC901 H64GX@ SD043100280	RC373 S32GX@ SD043100280	RC375 S32GX@ SD043100280	RC376 S32GX@ SD043100280	RC378 S32GX@ SD043100280	RC381 S32GX@ SD043100280	RC901 S32GX@ SD043100280
RC373 H32GX@ SD043100280	RC374 H32GX@ SD043100280	RC377 H32GX@ SD043100280	RC378 H32GX@ SD043100280	RC381 H32GX@ SD043100280	RC901 H32GX@ SD043100280						

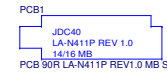
TPM Bom Option



VCORE_FW_ID



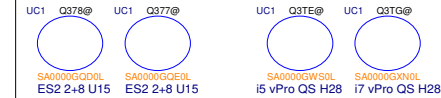
PCB



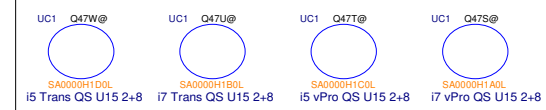
X76



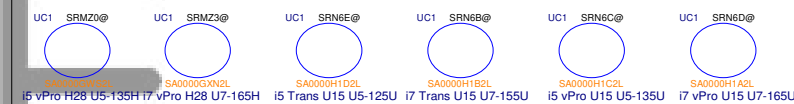
CPU DVT1



CPU DVT2



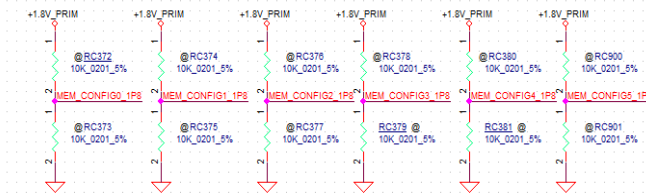
CPU A00

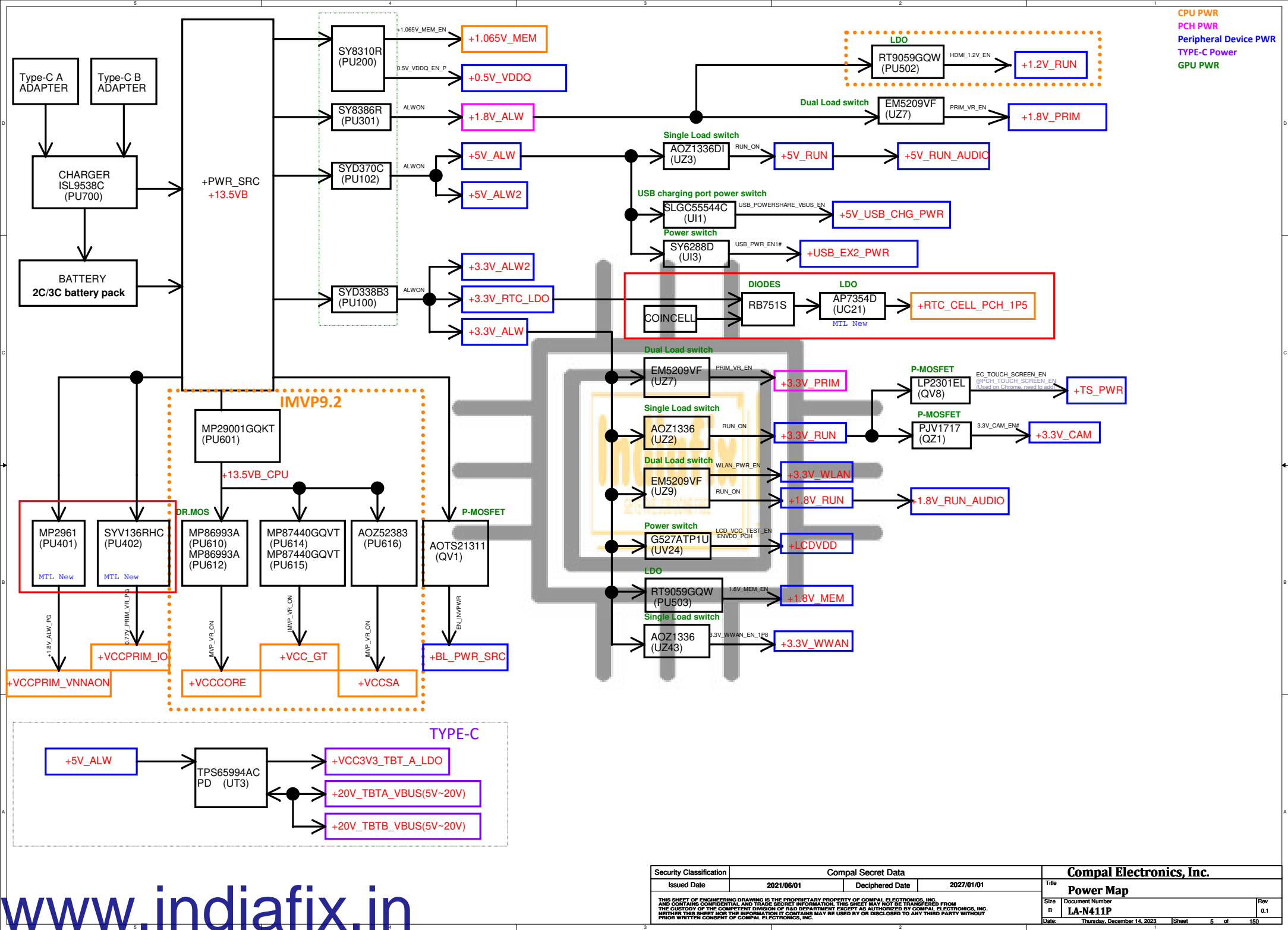


TBT Bypass path



DRAM Option Detail at Page 004



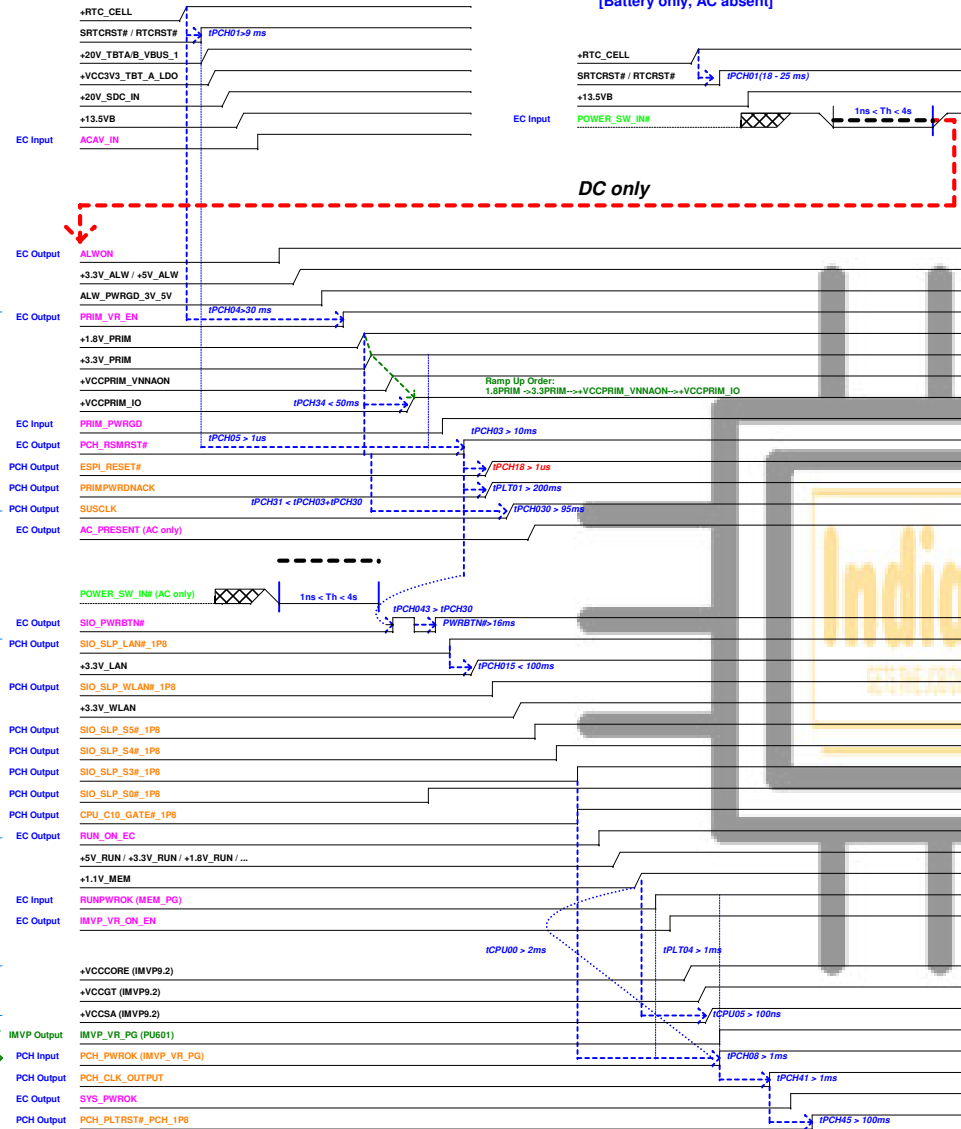


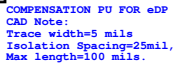
CPU PWR
PCH PWR
Peripheral Device PWR
TYPE-C Power
GPU PWR

Power Sequence G3 -> S0 Non deep

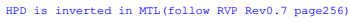
[AC in]

[Battery only, AC absent]





COMPENSATION PU FOR eDP
CAD Note:
Trace width=5 mils
Isolation Spacing=25mil,
Max length=100 mils.

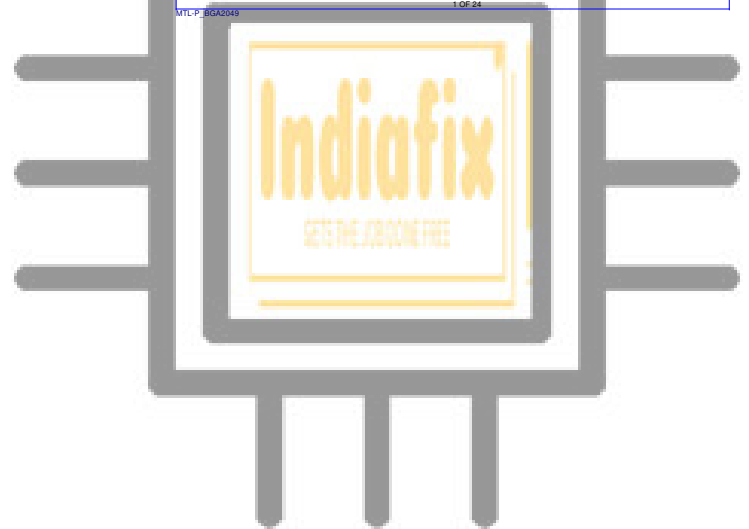


SKU	P Processor Line
DDI A	eDP**/MIPL_0
DDI B	eDP**/DP**/HDMI**/MIPL_1
TC90	
TC91	DP**, DPvC*, HDMI*
TC92	
TC93	

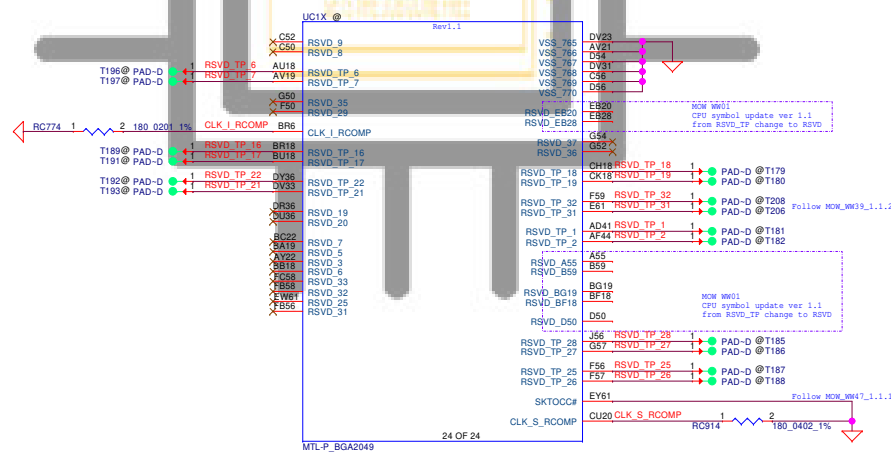
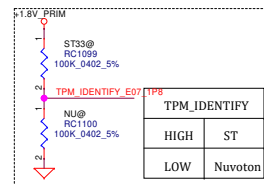
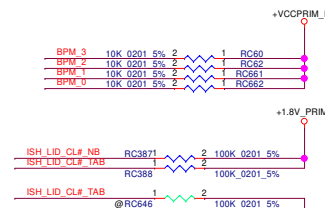
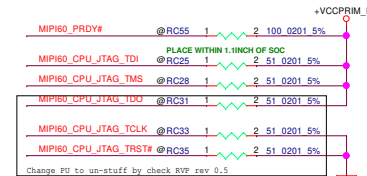
Note: MI6B3 supported on DDI with re-timer
Note: UM6B10 supported from TCP ports on DP connector only
Each of the TCP port can support DPvC* (DisplayPort** over Type-C).

Note: HBR3 supported on DDI with re-timer
Note: UHBR10 supported from TCP ports on I
Each of the TCP port can support DPoC* (Dis

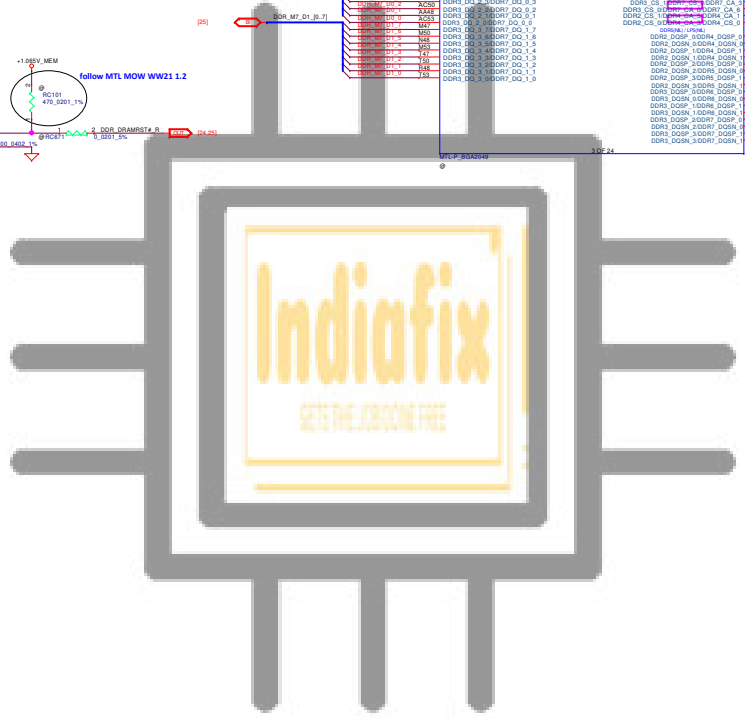
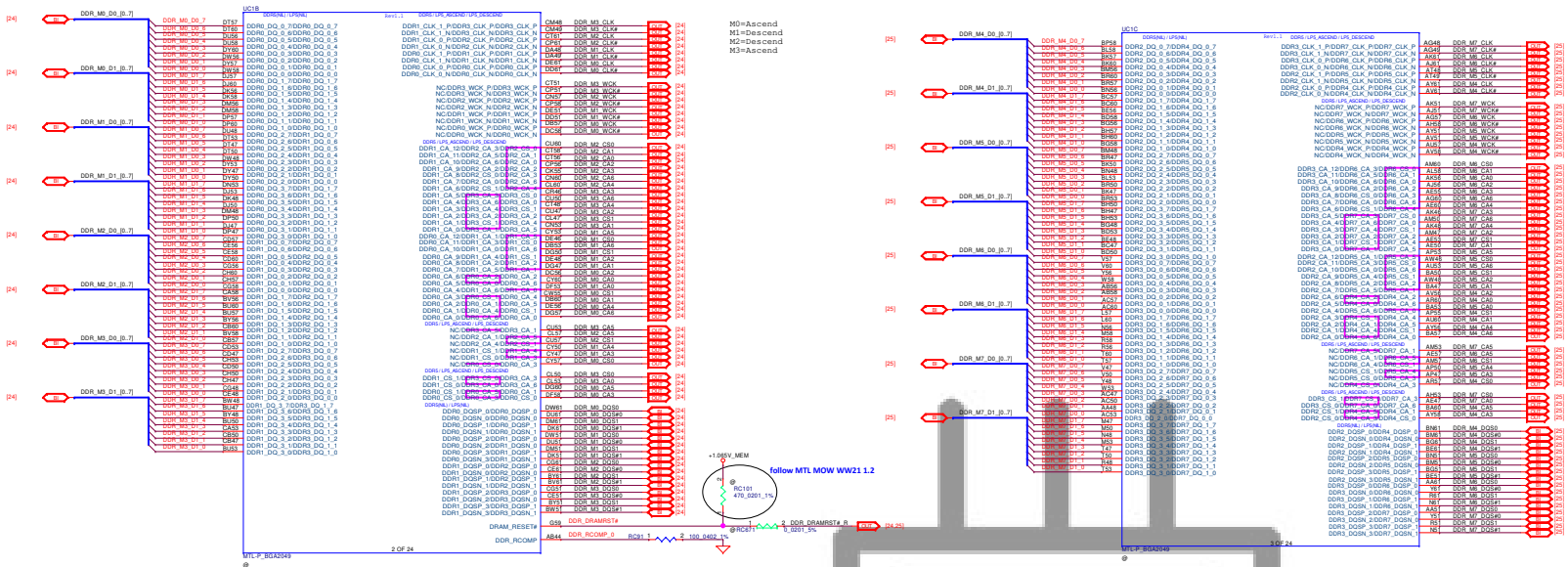
TBT_Port 2 : Front port



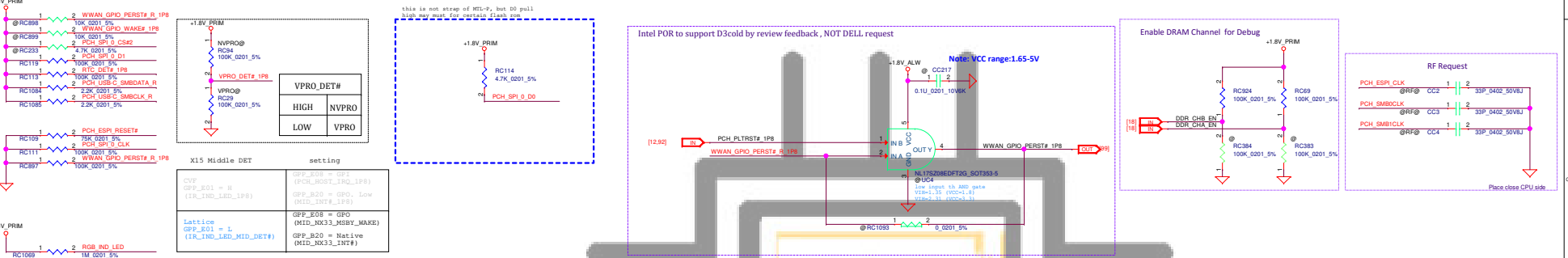
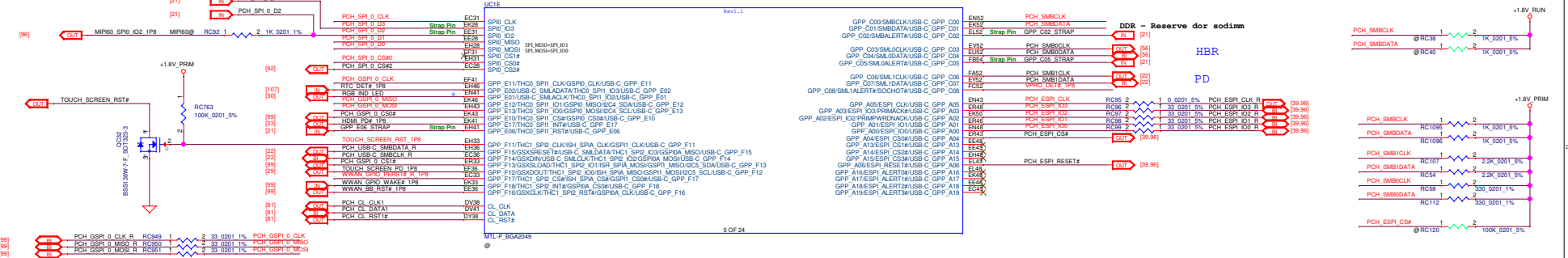
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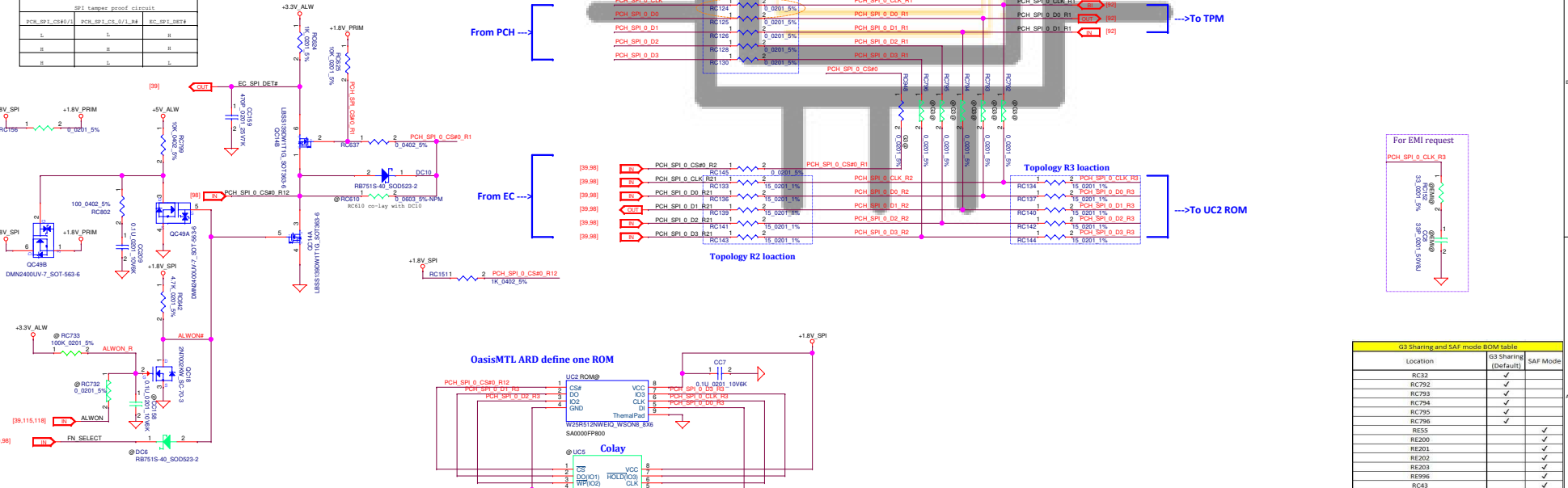


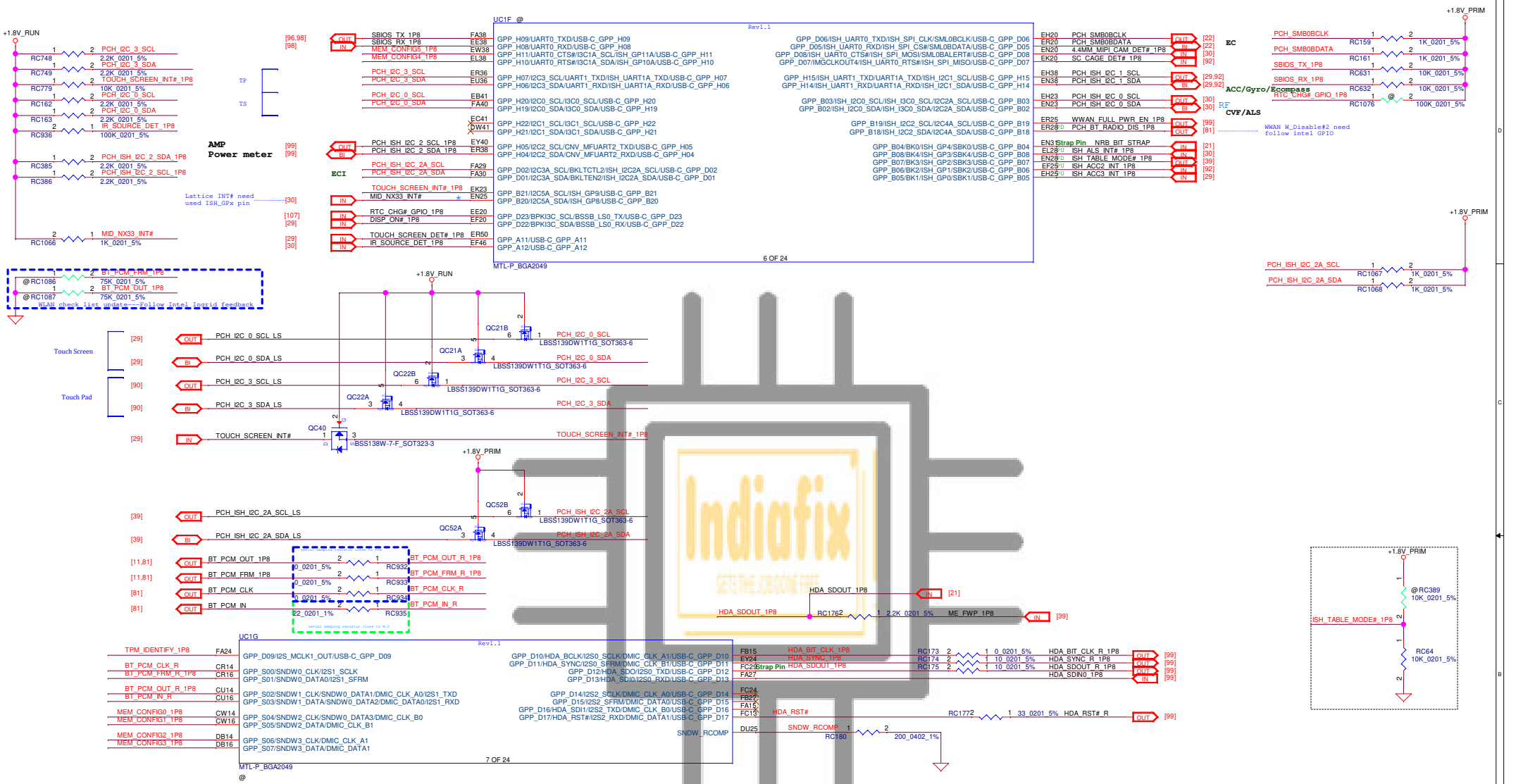
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Revision		Version		1.0	



EC G3 SPI Flash Sharing with Wire-OR(2 Flash and 1TPM)
Reference640982_MTL_P_PDG_Rev0p7.pdf
at P.428

SPI tamper proof circuit (Place on TOP side for secure consideration)





DRAM Option Detail at Page 004

Capacitor	Value	Capacitor	Value	Capacitor	Value	Capacitor	Value	Capacitor	Value	Capacitor	Value
@RC372	10K_0201_5%	@RC374	10K_0201_5%	@RC376	10K_0201_5%	@RC378	10K_0201_5%	@RC380	10K_0201_5%	@RC900	10K_0201_5%
@RC373	10K_0201_5%	@RC375	10K_0201_5%	@RC377	10K_0201_5%	@RC379	10K_0201_5%	@RC381	10K_0201_5%	@RC901	10K_0201_5%

RF Request. Place near CPU side (Intel MOV)

Component	Value	Component	Value	Component	Value
@RF@ CC33	2.2P_0201_50V8C	@RF@ CC34	2.2P_0201_50V8C	@RF@ CC35	47P_0201_50V8J

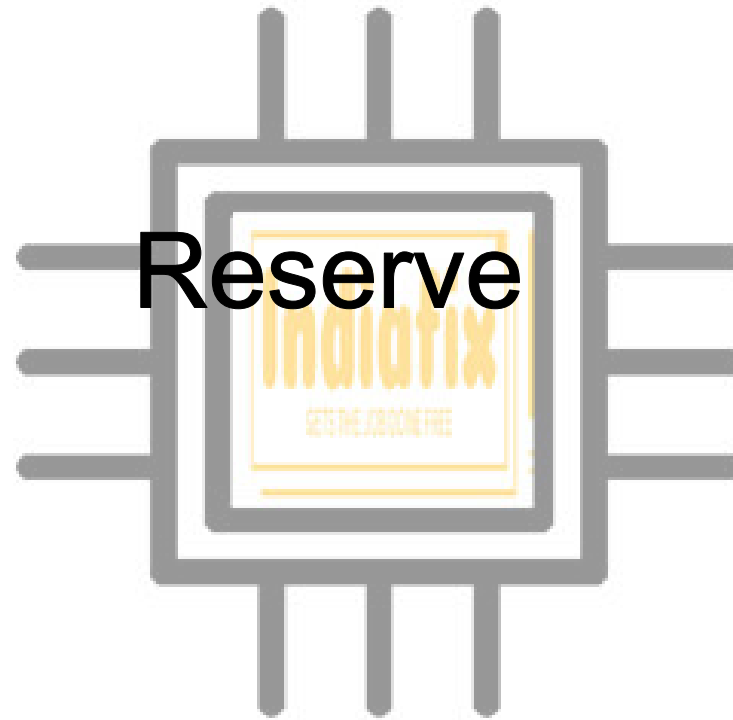
TPM_IDENTIFY	Value
HIGH	ST
LOW	Nuvoton

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Compal Electronics, Inc.	
SoC(5/14)HDA,SNDW	
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Oasis support PCIe Gen4

Card Reader
RTS5242

M.2 2230(WLAN) ---->

M.2 3042(WWAN) ---->

OasisMTL Drop

[81]
[81]
[81]
[81]

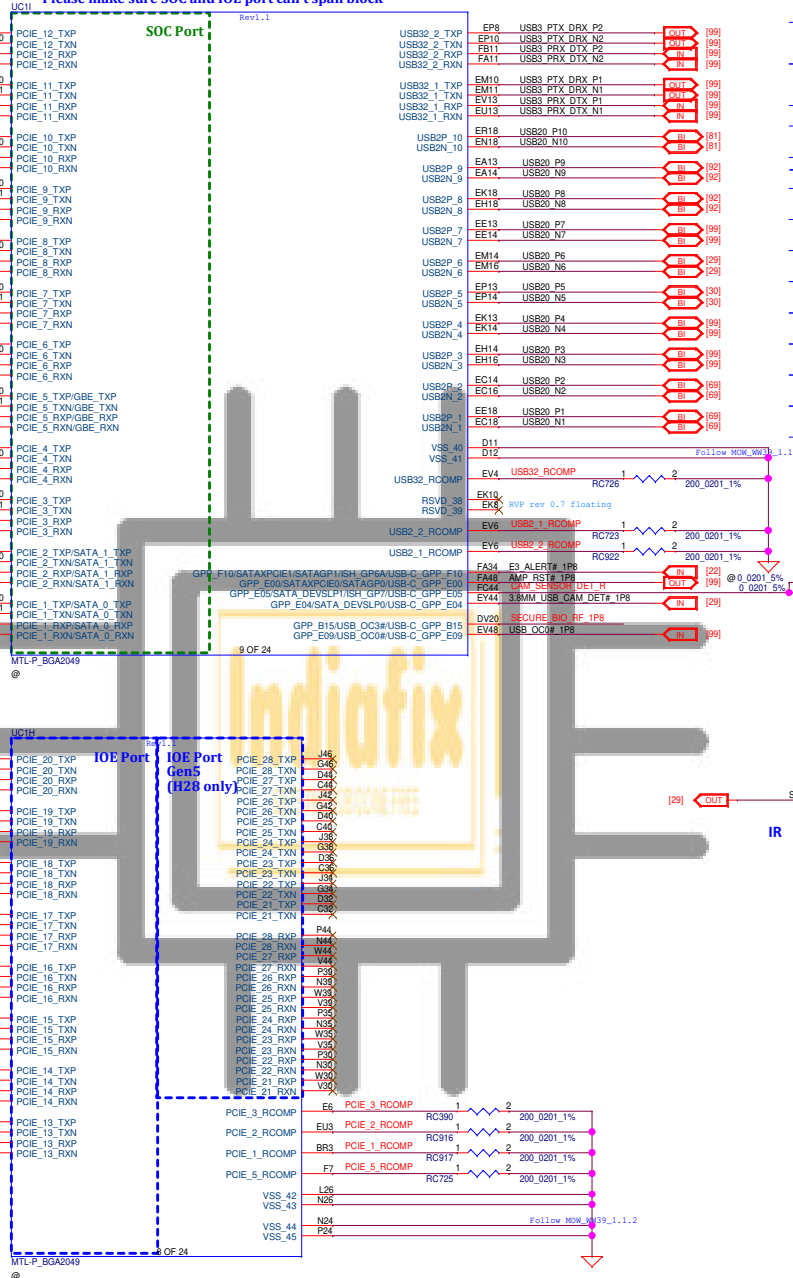
[99]
[99]
[99]
[99]

OasisMTL no RJ45

Lane reversed
For Layout & Length
limitation

M.2 2230 SSD
PCIe Gen4 x 4

SOC port CLKREQ# and CLKOUT[5:0], PCIe port [12:0]
IOE Port CLKREQ# and CLKOUT[8:6], PCIe port [20:13]
Please make sure SOC and IOE port can't span block



M.2 3042 (WWAN)

Ext USB3 Port 1 Charge

M.2 2230 (BT)

-----> Reserved FPR in PB

USH

M.2 3042 (WWAN)

Camera

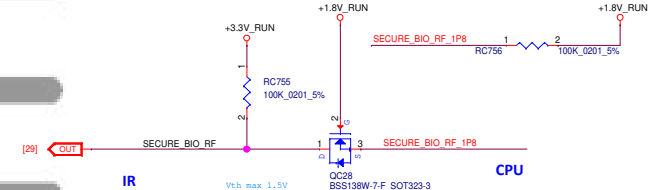
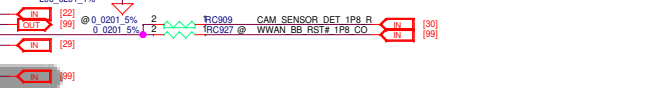
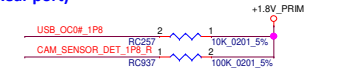
Camera MCU

Ext USB Port 2

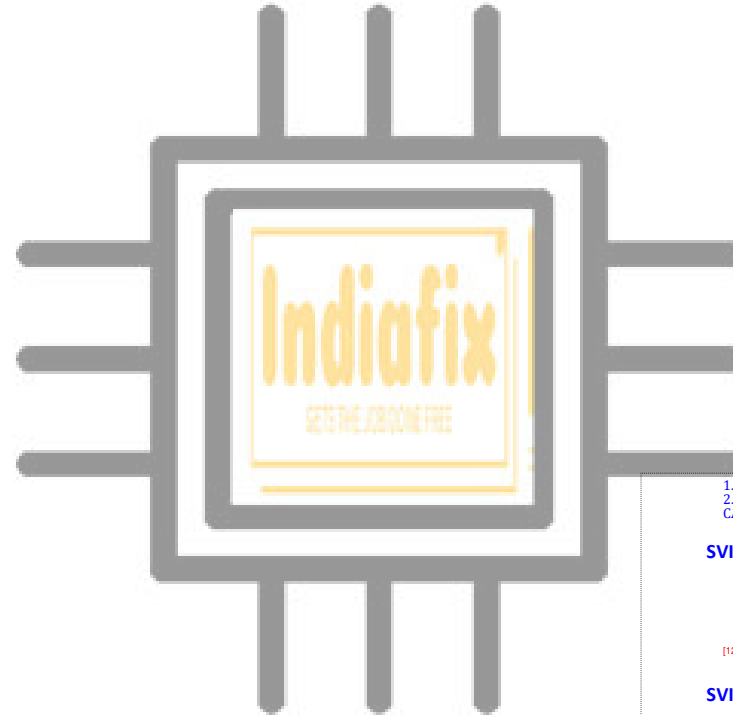
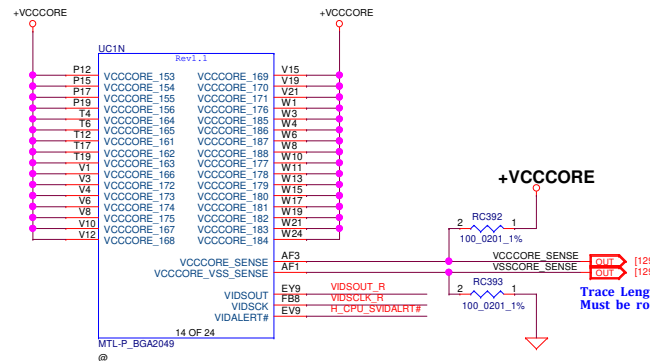
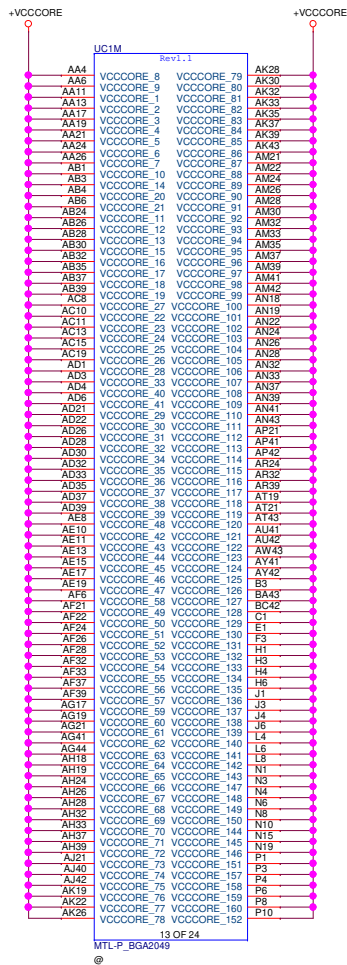
Ext USB Port 1 Charge

Type-C port 2 (Front port)

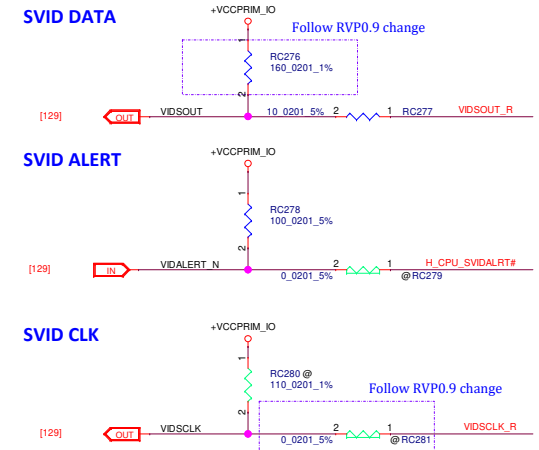
Type-C port 1 (Rear port)

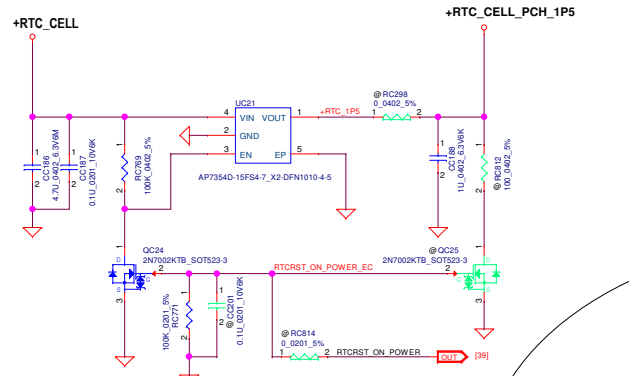
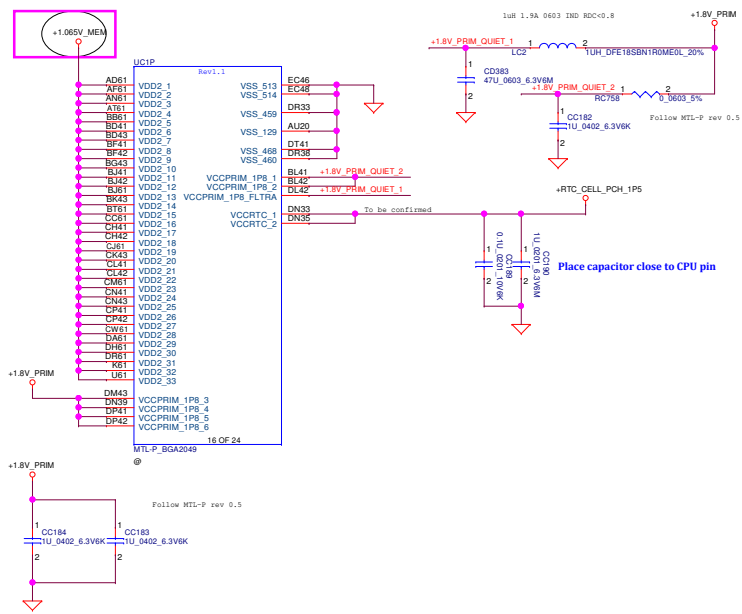


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				Rev	0.1
				Date:	Thursday, December 14, 2023
				Sheet	14 of 150

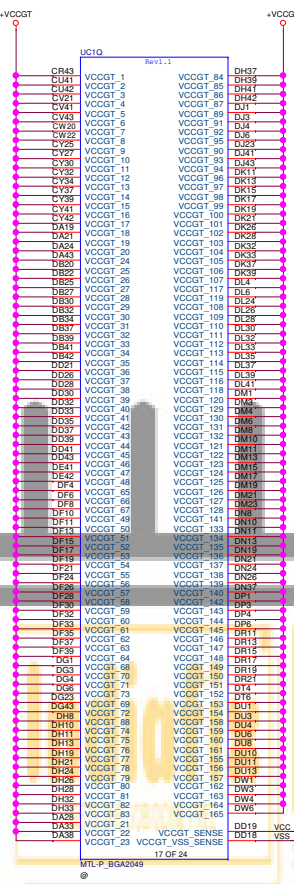
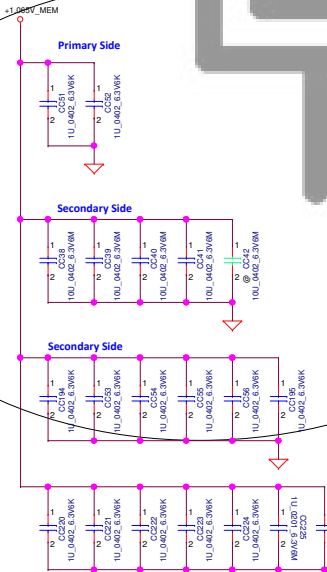


- 1.The total Length of Data and Clock (from CPU to each VR) must be equal (± 0.1 inch).
 - 2.Route the Alert signal between the Clock and the Data signals.
- CAD Note: Place the PU resistors close to CPU

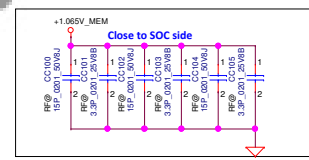




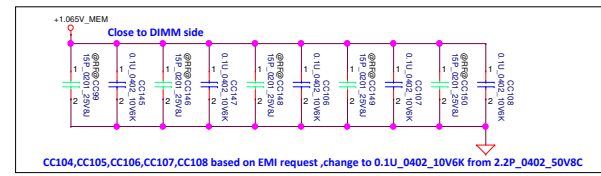
640982_MTL_UPH_PDG_Rev0p7
VDD2:
Primary Side cap
2 x 1uF 0402
Secondary side
3 x 10uF 0402 + 4 x 1uF 0402 +PH 1 x 10uF 0402



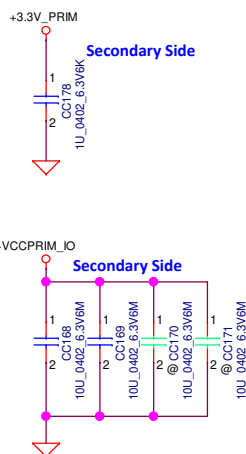
Load Regulation (ΔV _{OUT})	1mA ≤ I _{OUT} ≤ 150mA (All Versions Except 4.5V)	-40	—	40	mV
	1mA ≤ I _{OUT} ≤ 150mA (Applicable to 4.5V Version)	-55	—	55	mV
Short Circuit Current Limit (Note 7)	V _{OUT} = 0V	—	60	—	mA
Quiescent Current (Note 8)	I _{OUT} = 0mA	—	0.25	0.6	μA
I _{STANDBY}	Set EN Low, No Load	—	0.02	0.2	μA
Output Current	—	150	—	—	mA
EN Input Low Voltage	—	—	—	0.4	V
EN Input High Voltage	—	1.0	—	5.5	V
Active Output Discharge Resistance (Note 10)	V _{IN} = 4.0V, V _{EN} = 0V	—	35	—	Ω



627205_ADL_P_PDG_Rev0p81
DDR Power Plane RF cap Decoupling
Caps Qty reference RVP
633909_ADL_P_DDR4_SODIMM_1DPC_RVP_SCH_Rev0p6
PLACE <4MM FROM SOC VDDQ, WITH EACH PAIR <12MM APART

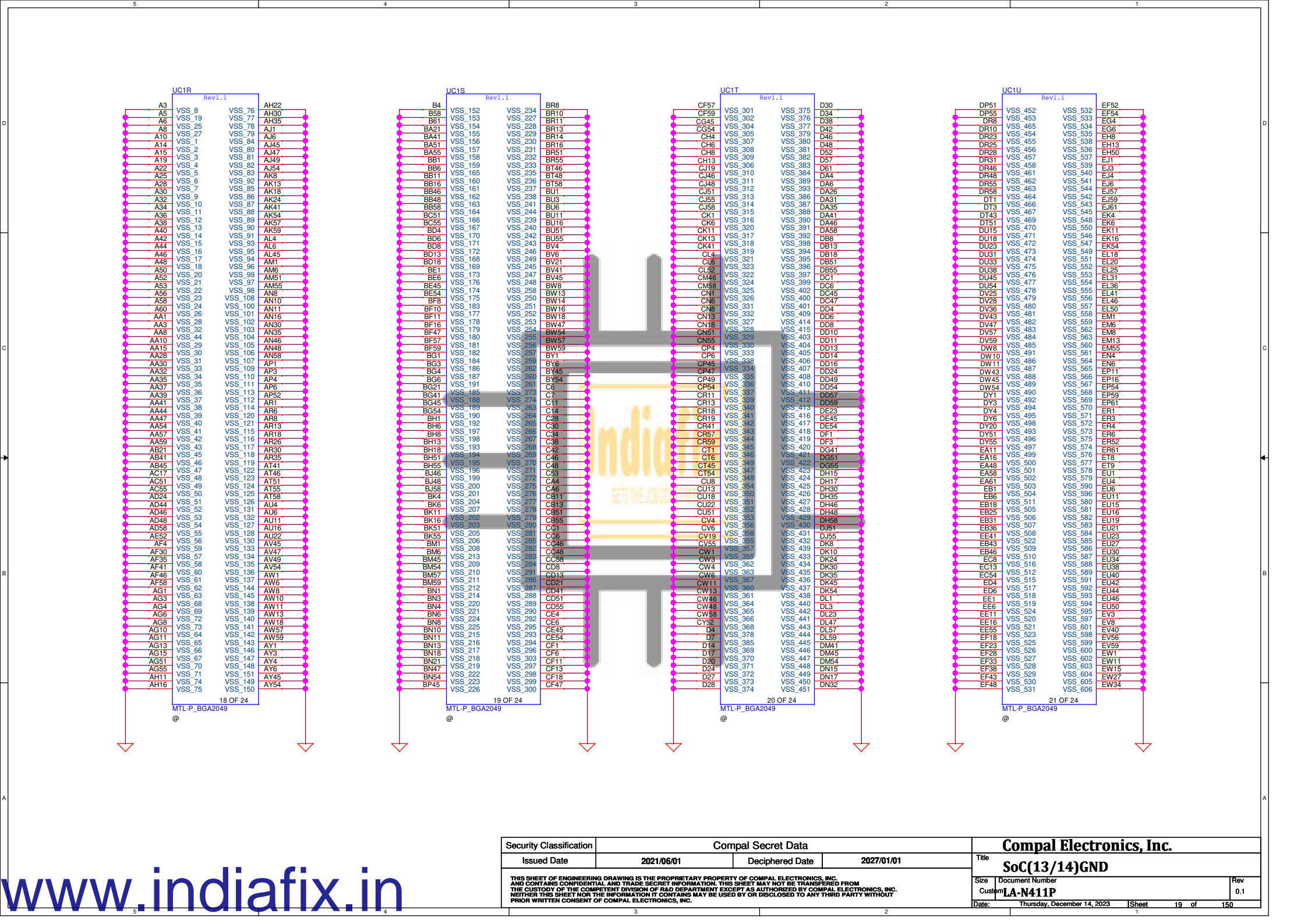


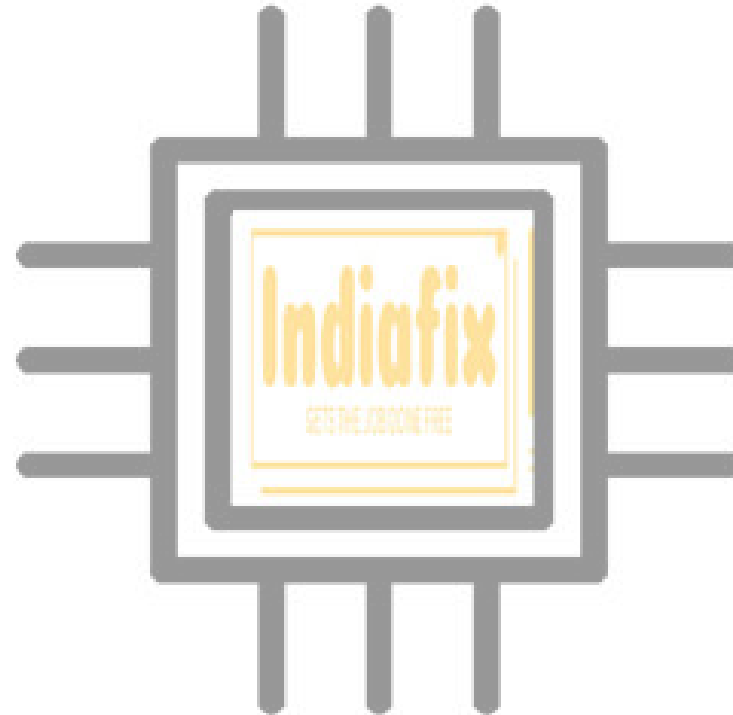
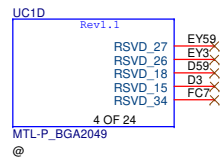
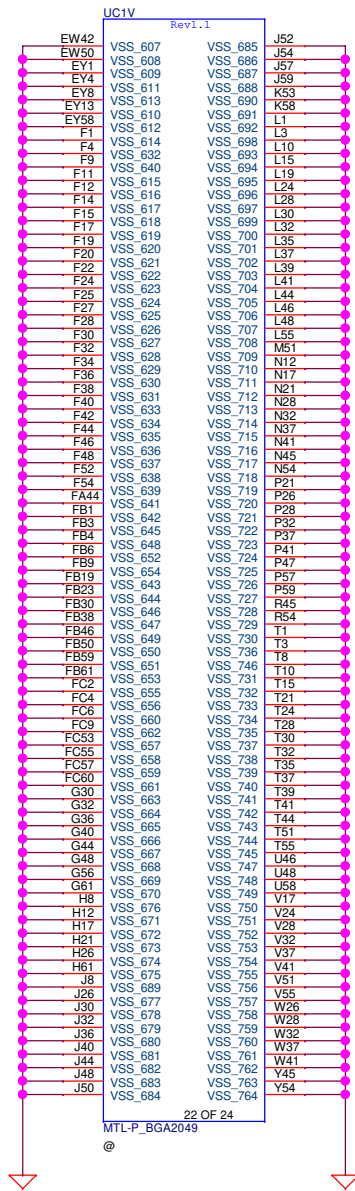
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Title	SoC(11/14)Power	Rev
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Reserved

This strap has a 20 kohm ± 30% internal pull-down. This strap should sample LOW. There should NOT be any onboard device driving it to opposite direction during strap sampling.
Note: The internal pull-down is disabled after RSMRST# deasserts.

Enable/Disable SPI Flash Descriptor Recovery

This strap has a 20 kohm ± 30% internal pull-down. Flash Descriptor Recovery for NIST SP800-193
0 - Flash descriptor recovery disable (Default)
1 - Flash descriptor recovery enable
Note: The internal pull-down is disabled after RSMRST# deasserts.

eSPI Flash Sharing Mode

This strap has a 20 kohm ± 30% internal pull-down.
• 0 => Host Attached Flash Sharing (aka MAFS) enabled (Default).
• 1 => Device Attached Flash Sharing (aka SAFS) enabled
Note: The internal pull-down is disabled after RSMRST# deasserts

Reserved

This strap has a 20 kohm ± 30% internal pull-down. This strap should sample LOW. There should NOT be any onboard device driving it to opposite direction during strap sampling.
Note: The internal pull-down is disabled after RSMRST# deasserts.

Reserved

DBG_PMODE (Internal 20 K Pull UP)

This strap has a 20 kohm ± 30% internal pull-up.

CCD Interface Default (Baltic Peak I3C or BSSB-LS)

This strap has a 20 kohm ± 30% internal pull-up.
• 0 => BSSB-LS is the default CCD interface.
• 1 => Baltic Peak I3C slave is the default CCD interface (Default).
Note: The internal pull-up is disabled after RSMRST# deasserts.

SVID VR Support

GPP_F20 (Weak internal PD 20K)

This strap has a 20 kohm ± 30% internal pull-down.
• 0 => VR(s) supporting SVID protocol is/are present.
• 1 => No VR supporting SVID is present. SoC will not generate (or respond to) SVID activity.
Note: The internal pull-down is disabled after RSMRST# deasserts

Reserved

This strap has a 20 kohm ± 30% internal pull-down. This strap should sample LOW. There should NOT be any onboard device driving it to opposite direction during strap sampling.
Note: The internal pull-down is disabled after RSMRST# deasserts.

Reserved Straps pin

This strap has a 20 kohm ± 30% internal pull-up.

Reserved Straps pin

This strap has a 20 kohm ± 30% internal pull-up.

JTAG ODT Disable

5/12 River eds 07 p55
The internal pull-up is disabled after RSMRST# deasserts

WEAK INTERNAL PD 20K

TLS Confidentiality

HIGH
LOW(DEFAULT) DISABLE

eSPI Disable

WEAK INTERNAL PD 20K
This strap has a 20 kohm ± 30% internal pull-down.
• 0 = Enable eSPI (Default)
• 1 = Disable eSPI
Note: The internal pull-down is disabled after RSMRST# deassert.

[11]

WEAK INTERNAL PD 20K

No Reboot

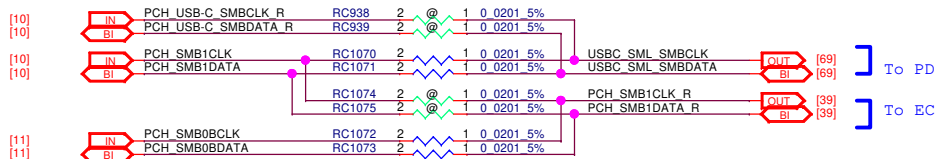
HIGH
LOW(DEFAULT) DISABLE NO REBOOT

FLASH Descriptor Security override

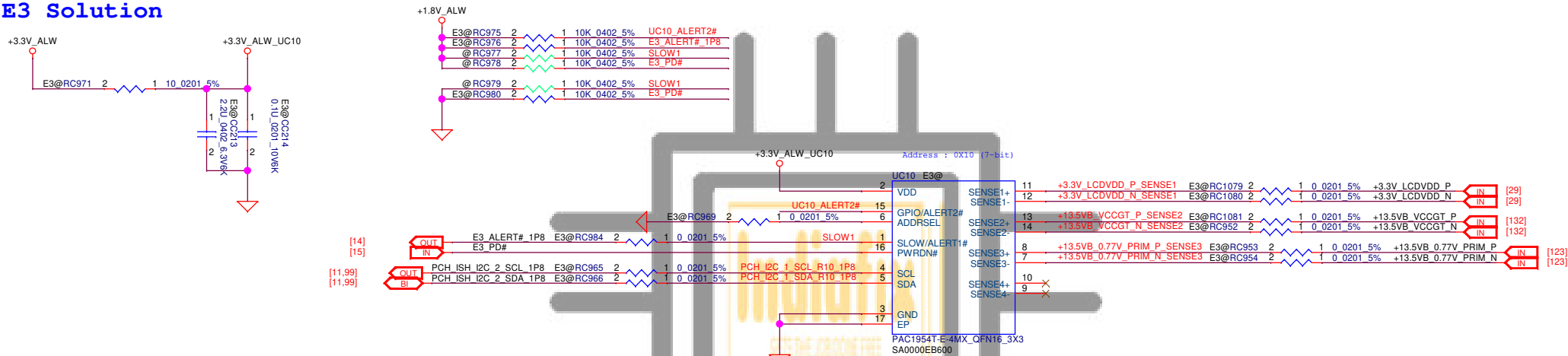
HIGH
LOW(DEFAULT) DISABLE

[11]

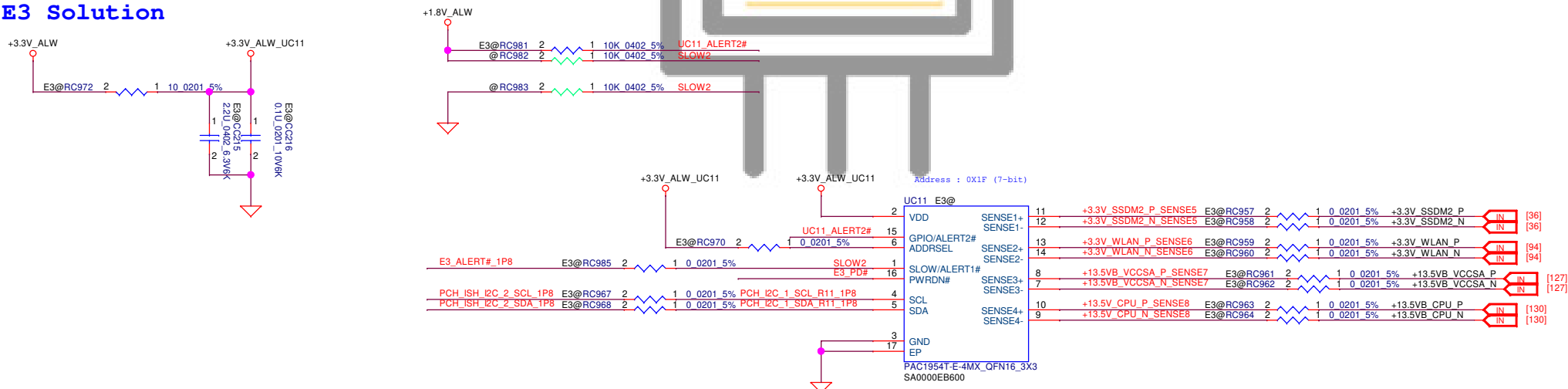
For vPro Docking support



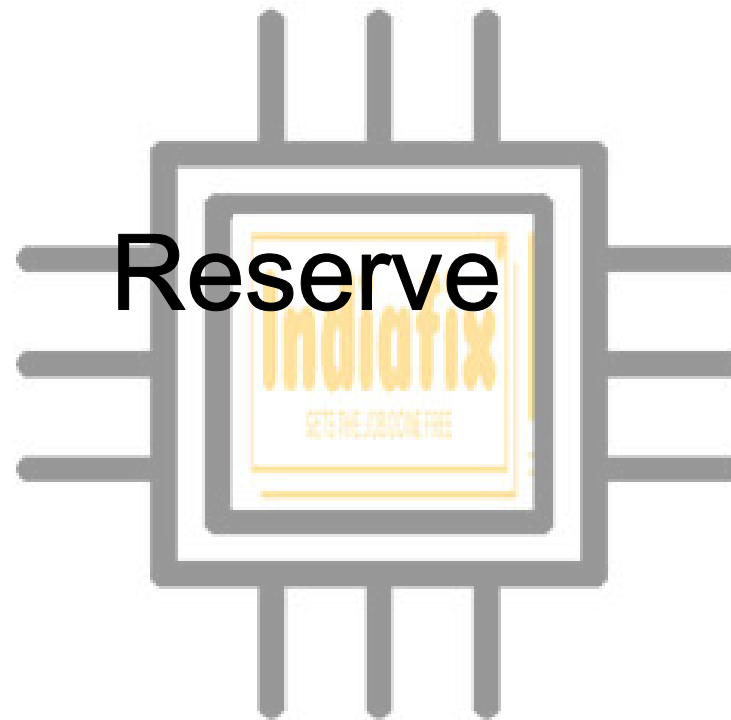
E3 Solution



E3 Solution

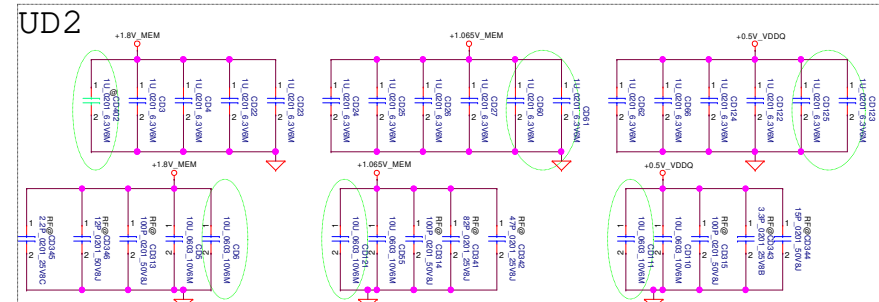
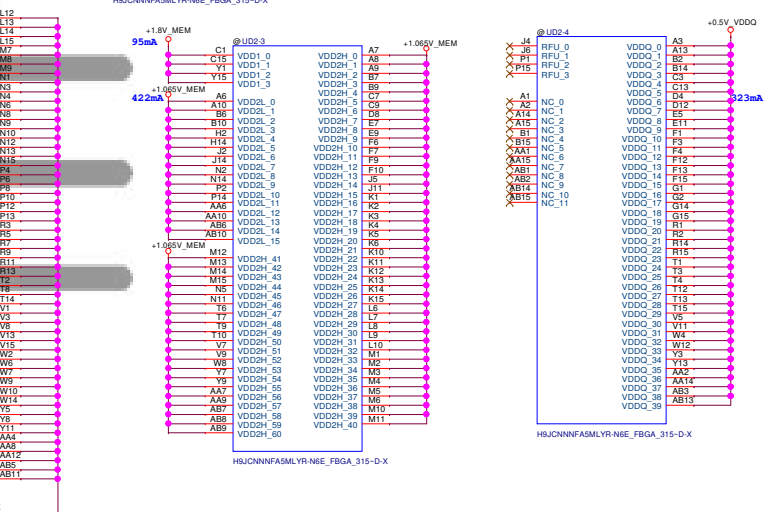
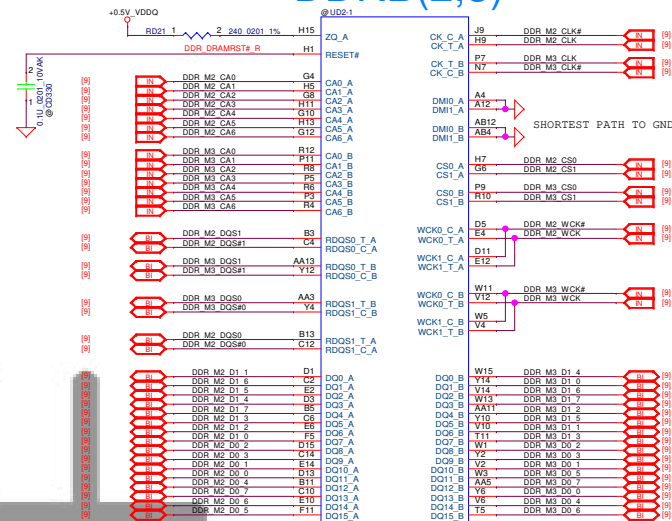


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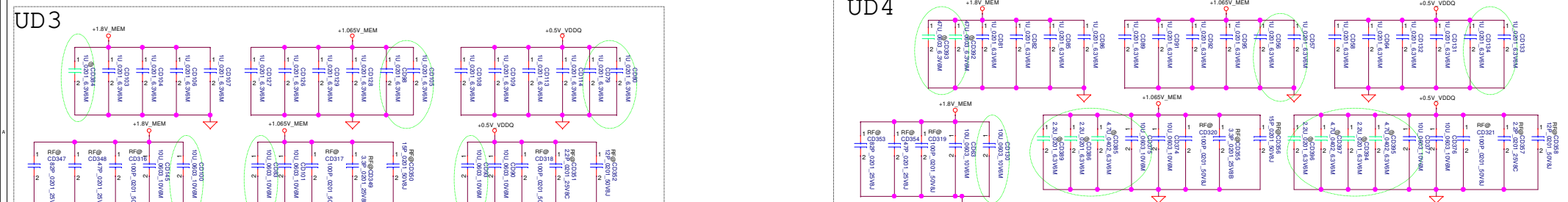
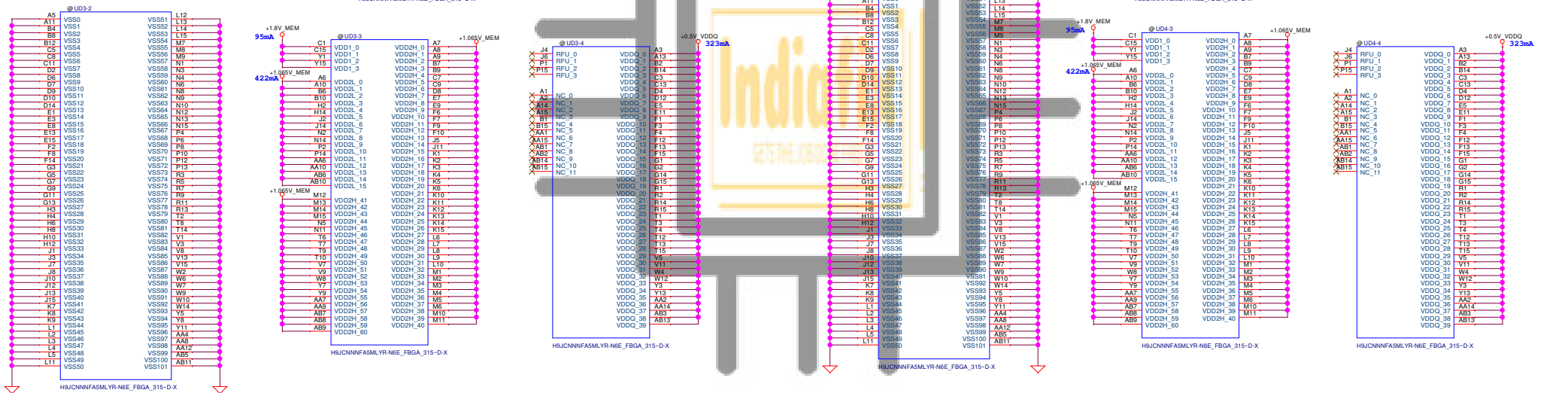
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DDRB(2,3)



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DDRD(6,7)



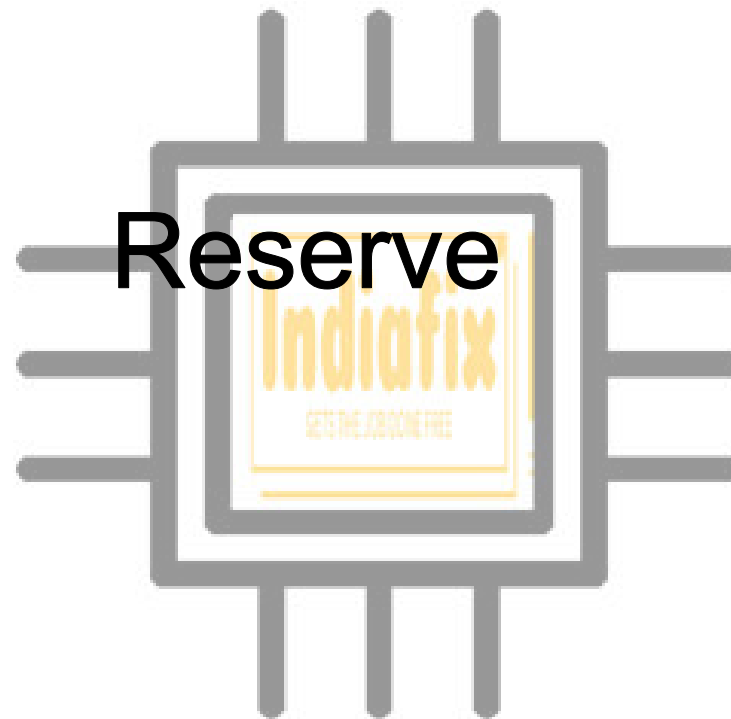
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Reserve

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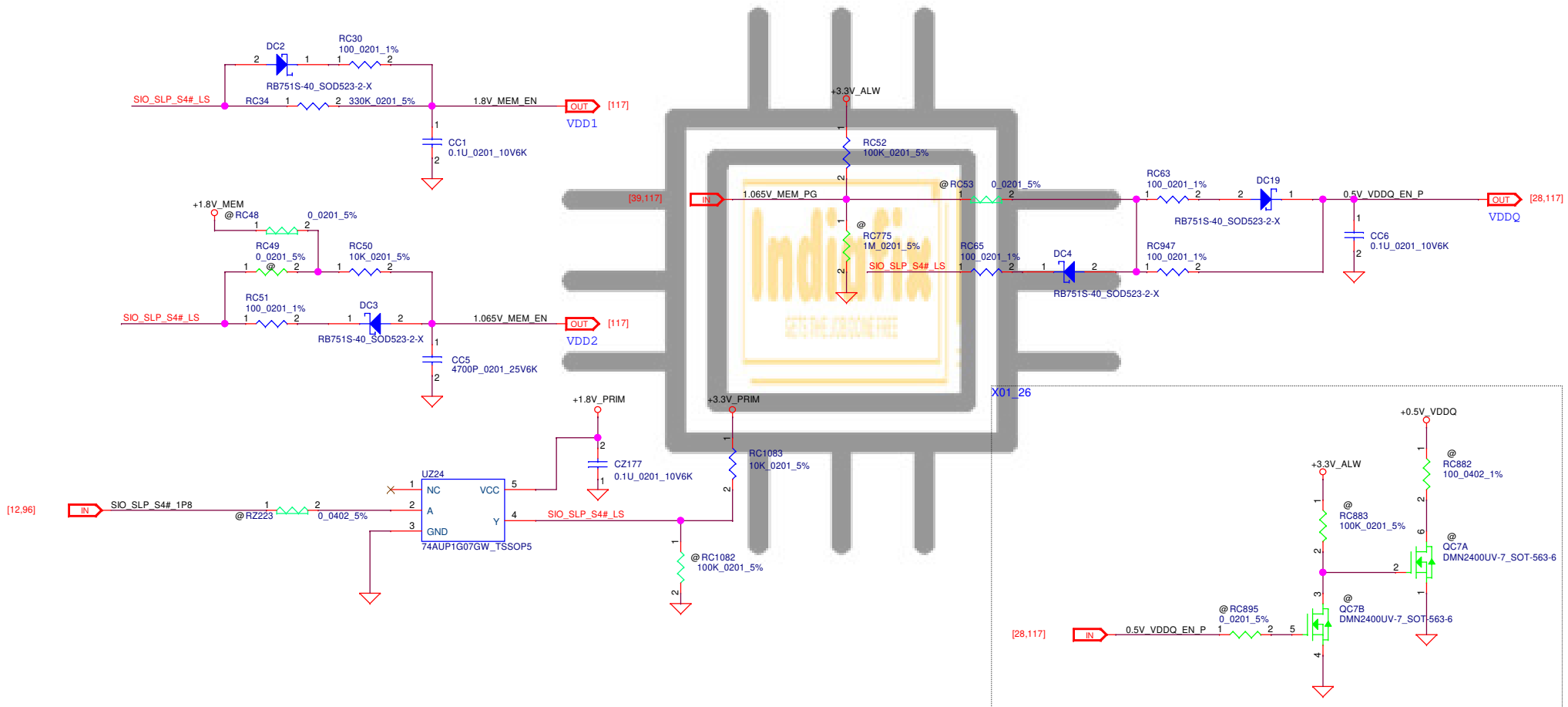
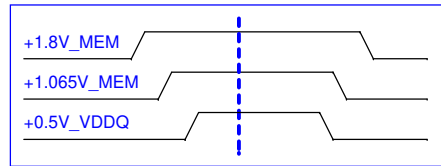
for DET review only

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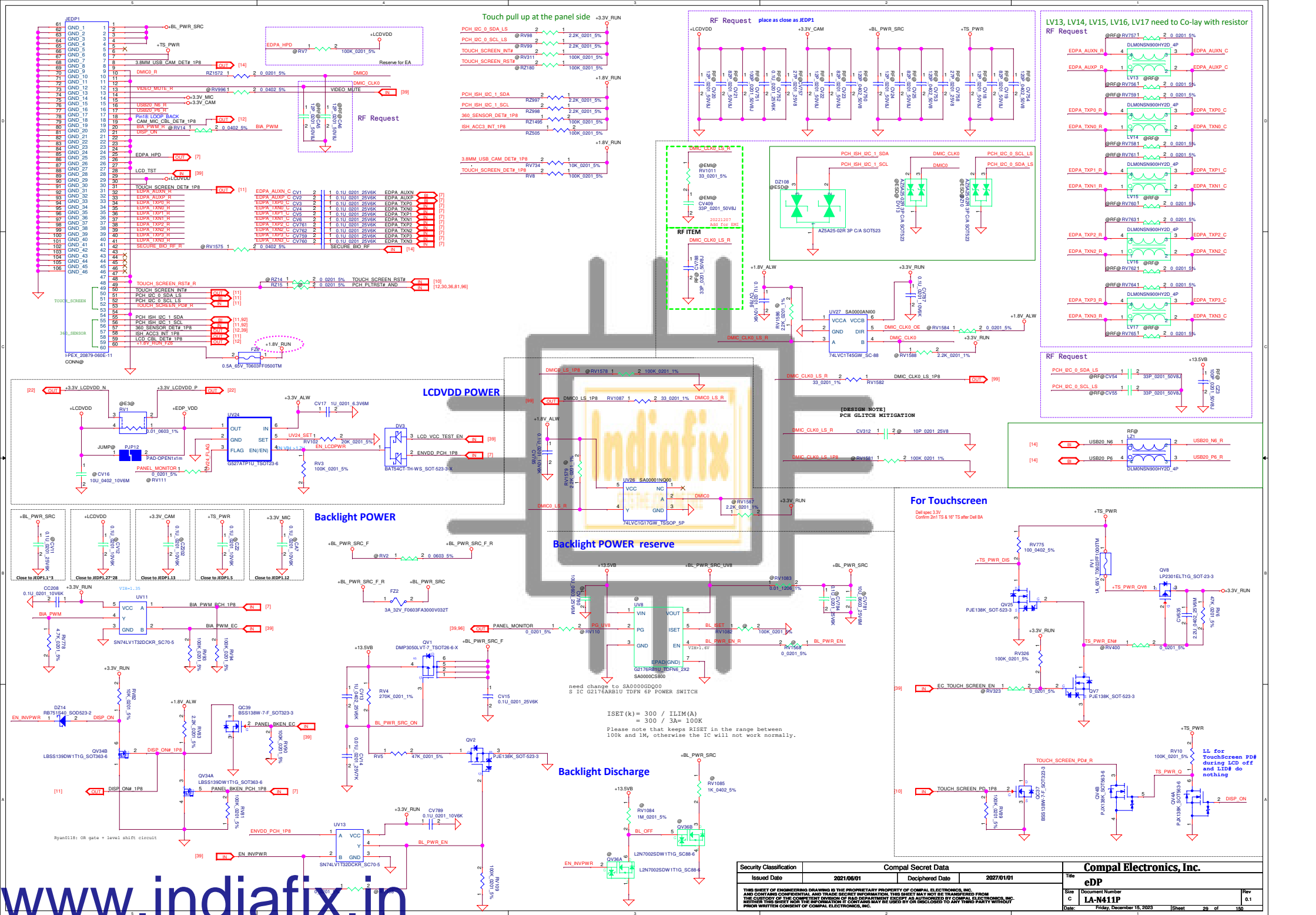


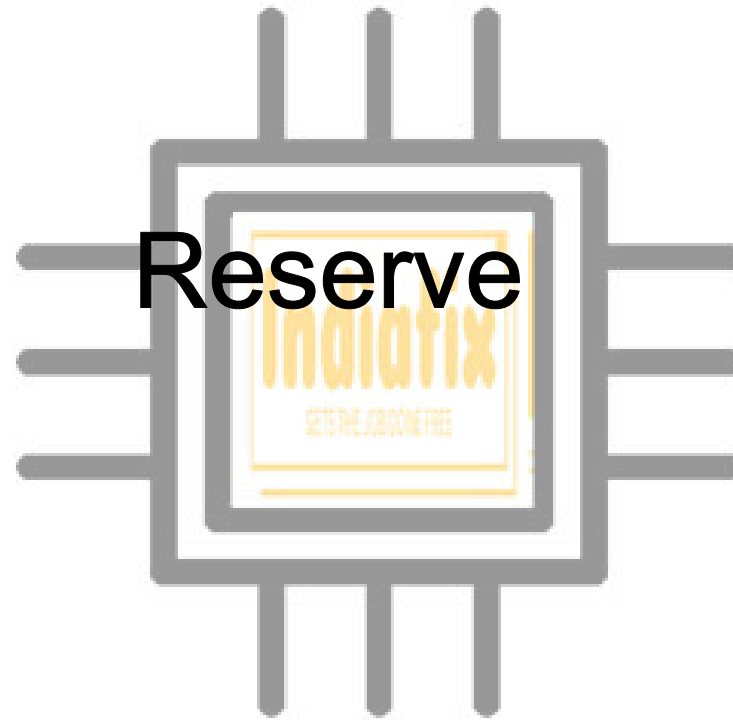
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Follow Intel RVP for LP5 sequence



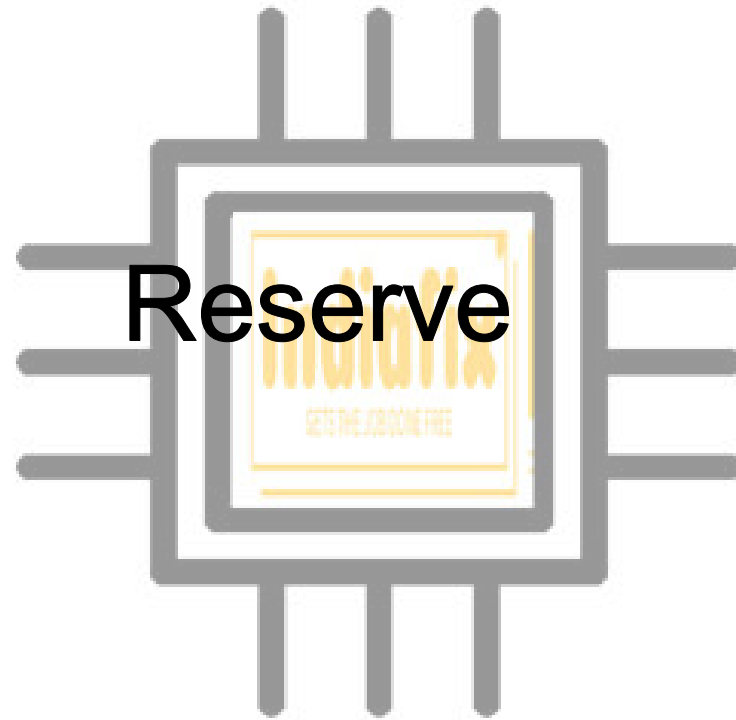
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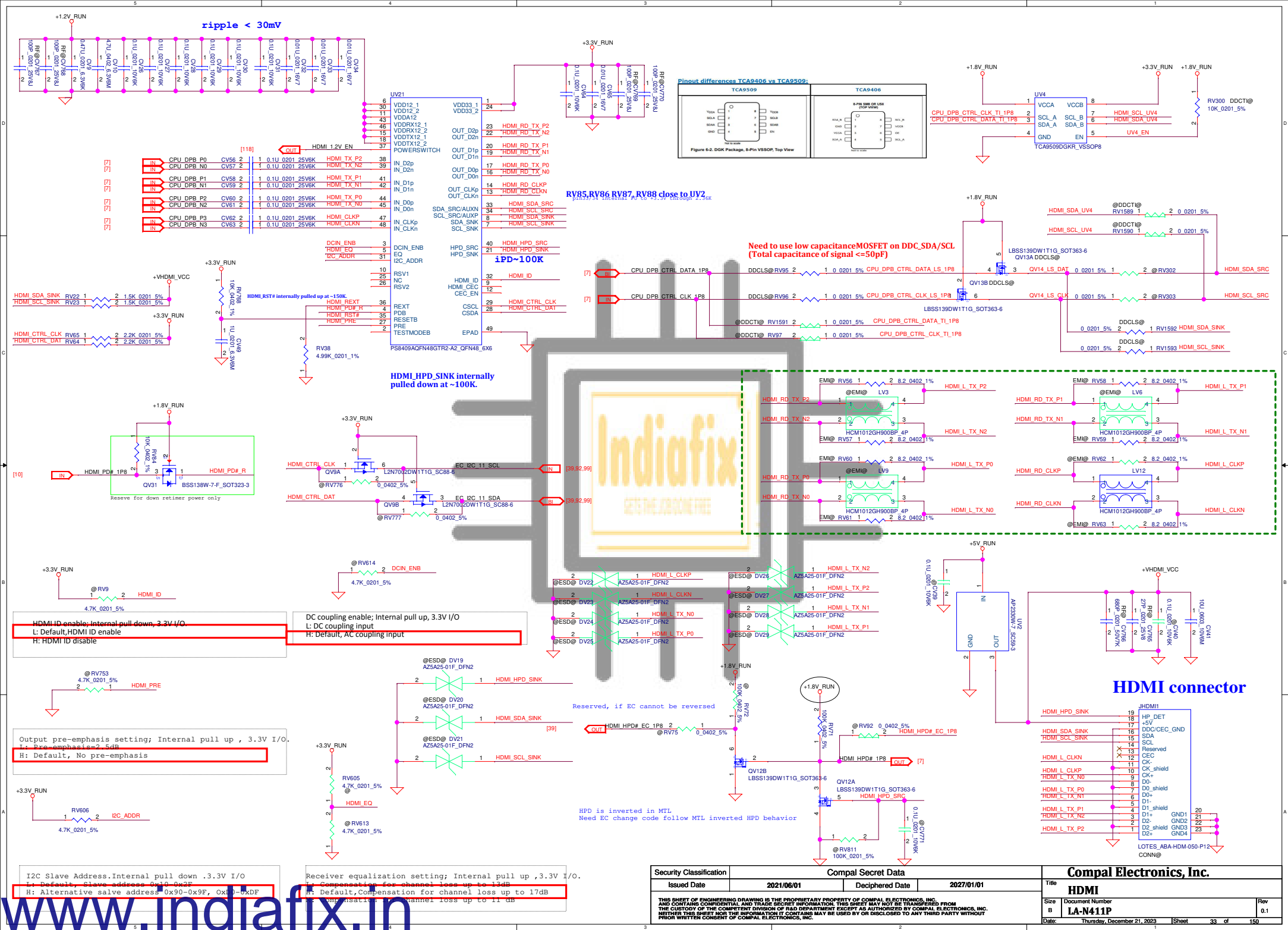


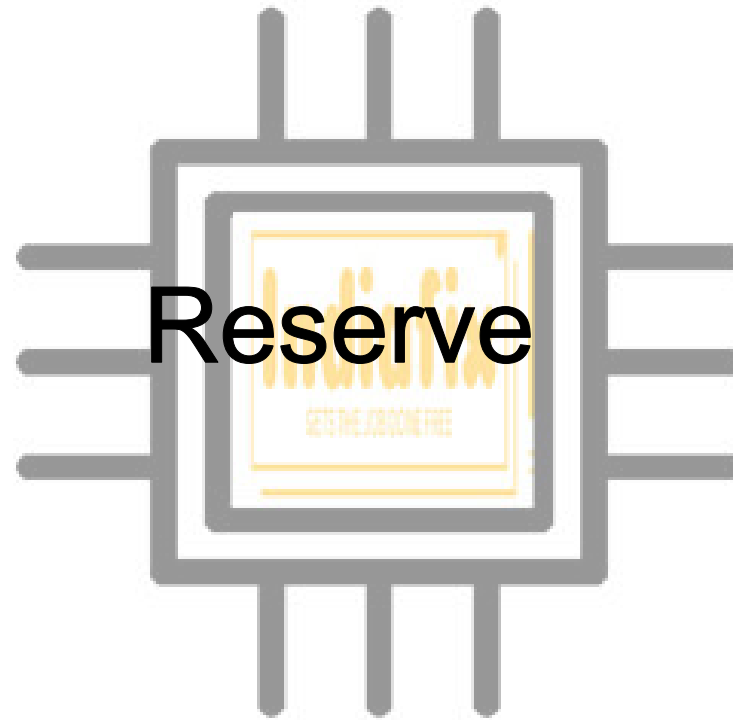
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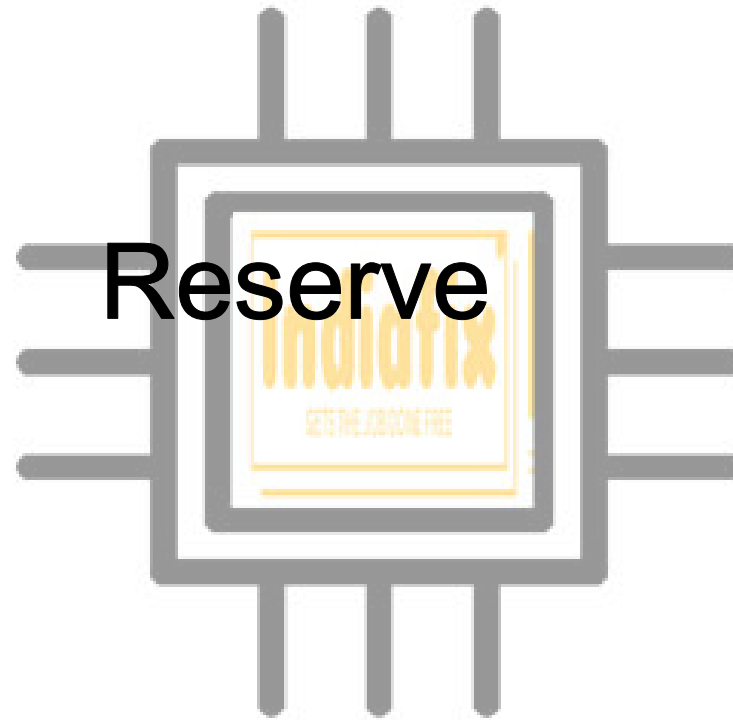
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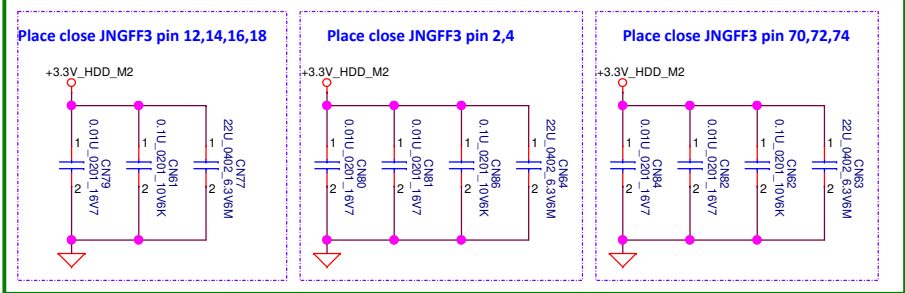
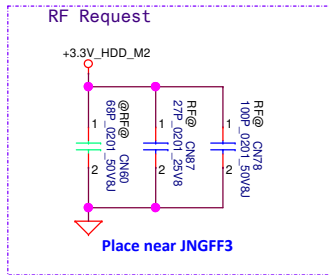
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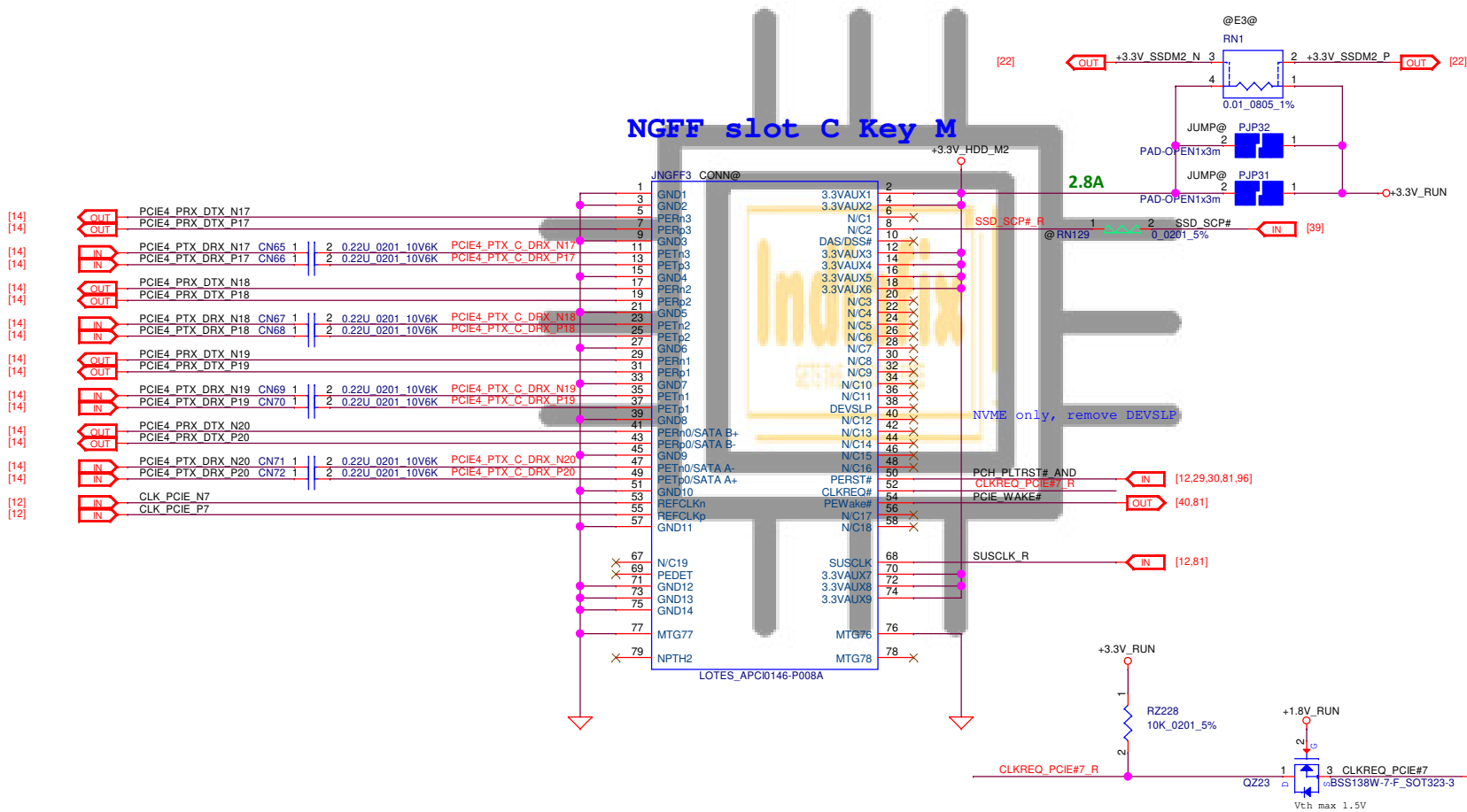


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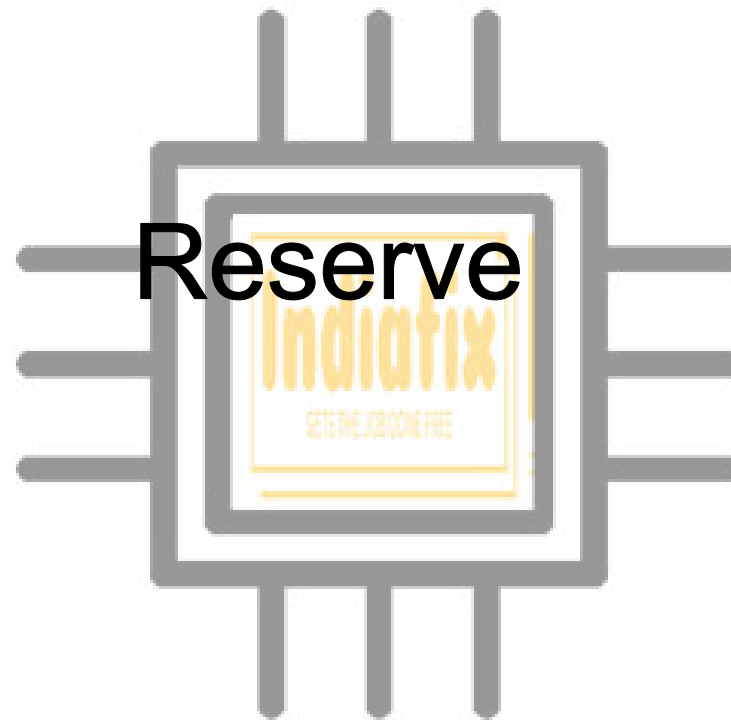
Add Power Decoupling for support Intel Teton Glacier



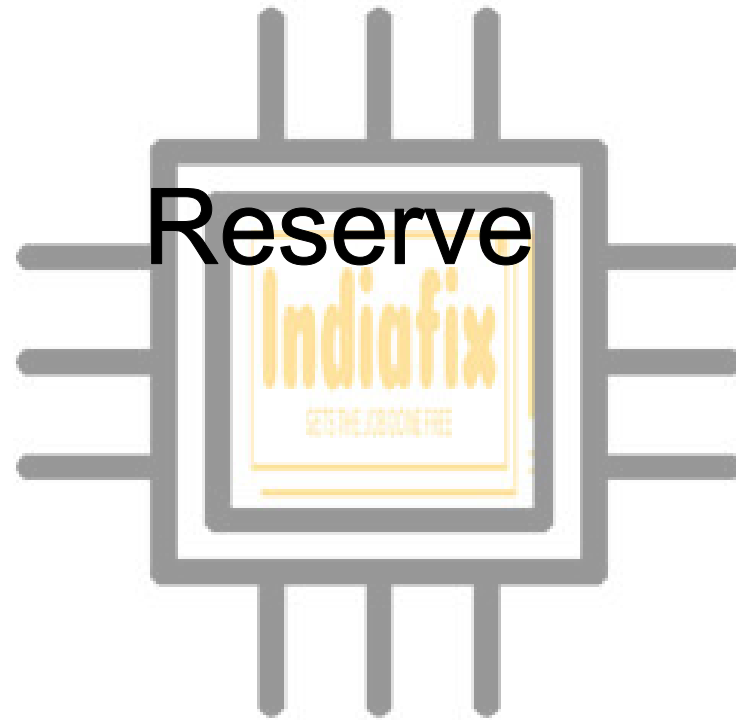
2230 SSD



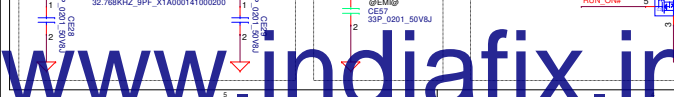
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Issued Date	2021/06/01	Deciphered Date	2027/01/01	Title	SSD & Re-Driver
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				Date:	Friday, December 15, 2023
				Sheet	36 of 150



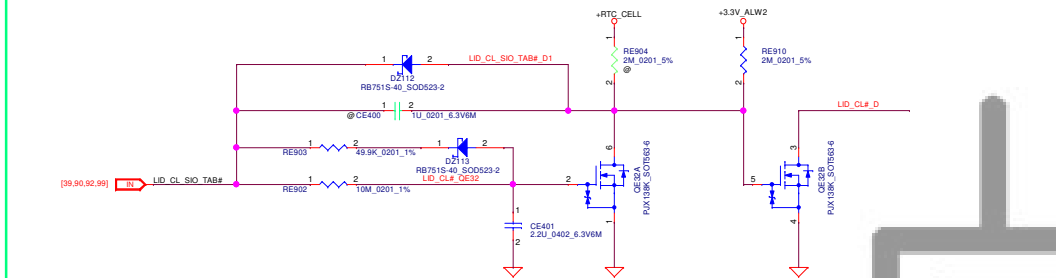
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Issued Date		2021/06/01	Deciphered Date	2027/01/01	Title
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		Size	Document Number	LA-N411P	0.1
Date:		Thursday, December 14, 2023	Sheet	37	of 150



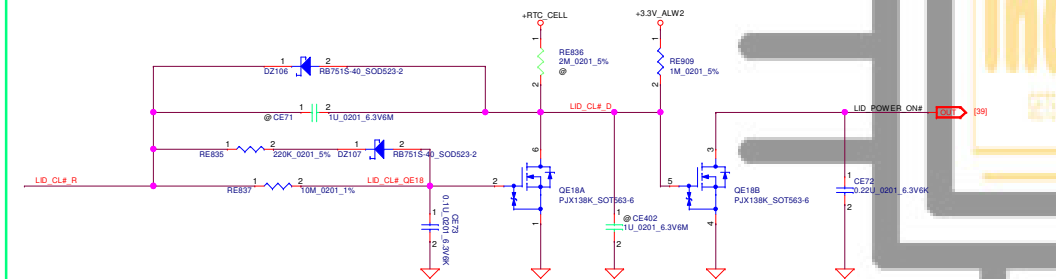
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Issued Date	2021/06/01	Deciphered Date	2027/01/01	Title	eMMC / UFS	
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				B	LA-N411P	0.1
				Date:	Thursday, December 14, 2023	Sheet 38 of 150



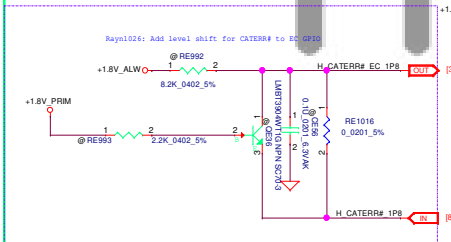
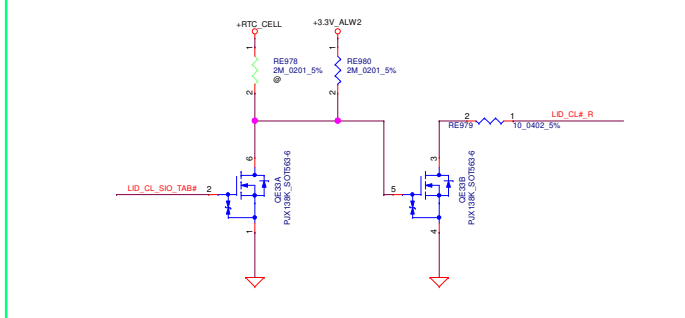
Fixed 360 auto power on



S5 LID OPEN POWER ON(Other Solution)



Fixed 360 auto power on Part2

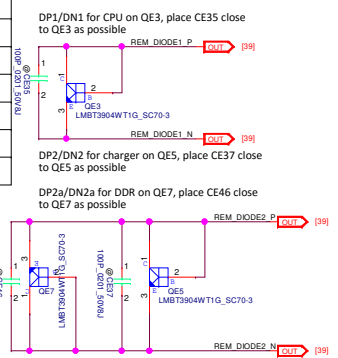


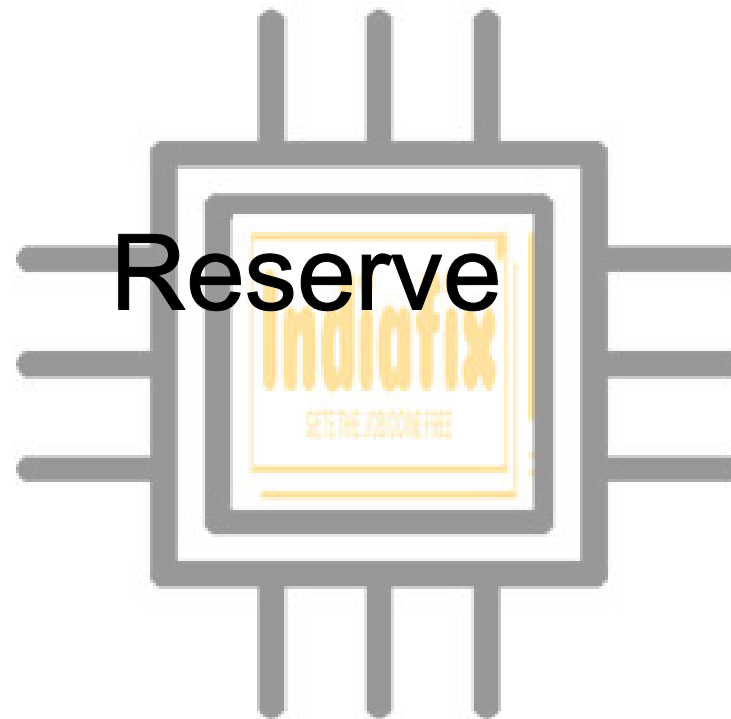
RE343	CE62	X14	7000
240K	4700p	Oasis	U15
130K	4700p	Oasis	H28
62K	4700p		
33K	4700p		
8.2K	4700p		
4.3K	4700p		
2K	4700p		
1K	4700p		

RE79	CE40	REV
240K	4700p	X00
130K	4700p	X01
62K	4700p	X02
33K	4700p	X03
8.2K	4700p	reserved
4.3K	4700p	A00
2K	4700p	
1K	4700p	

Thermal diode mapping

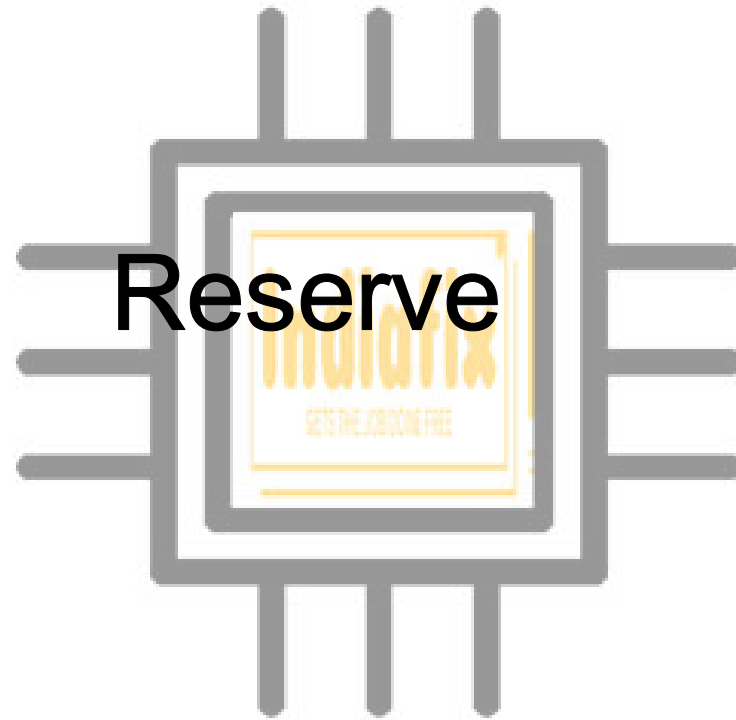
5200 Channel	Location
DP1/DN1	CPU (QE3)
DP2/DN2	Skin Sensor (QE5)
DP2a/DN2a	Ambient (QE7)
DP3/DN3	CPU VR (QE13)
DP3a/DN3a	Charge (QE14)
DP4/DN4	DDR (QE6)



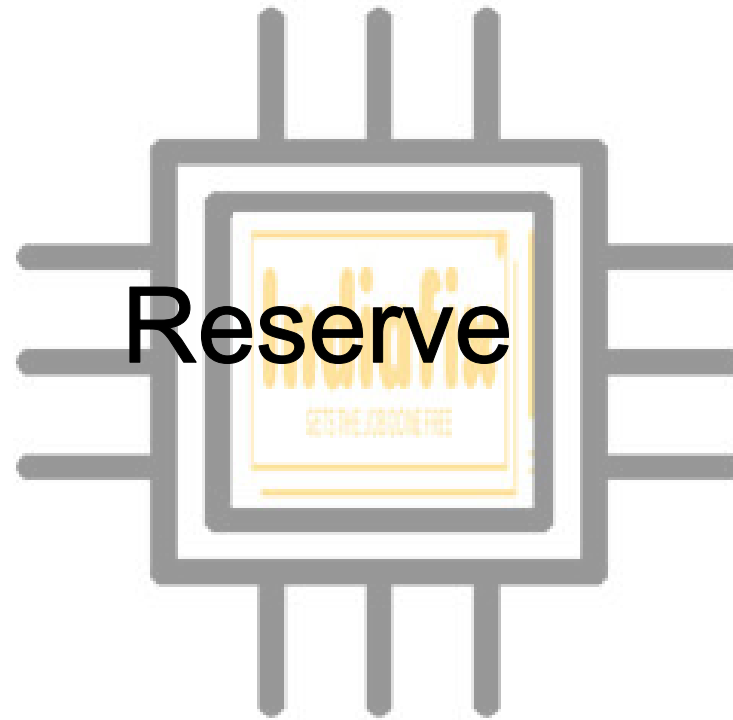


Reserve

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				Date:	Thursday, December 14, 2023
				Sheet	41 of 150

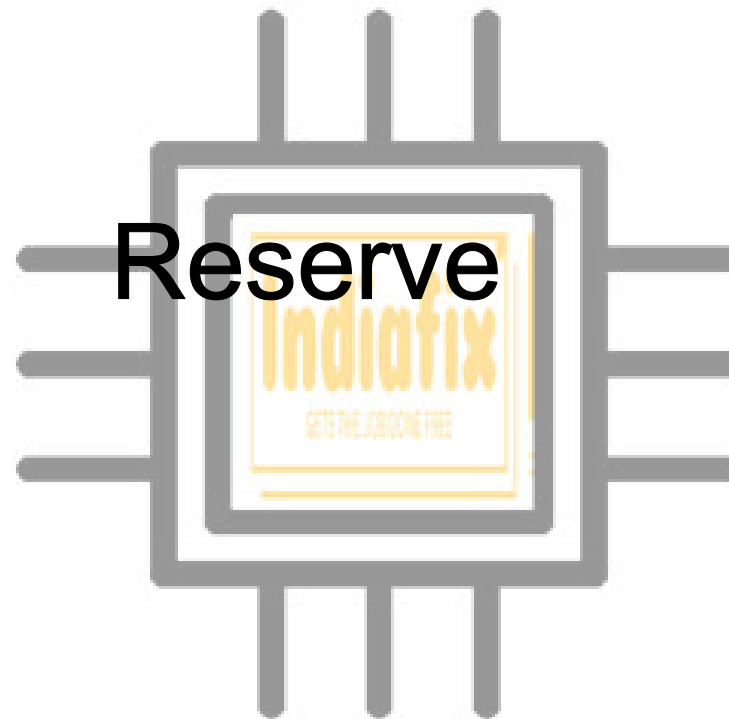


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				Sheet 42	of 150

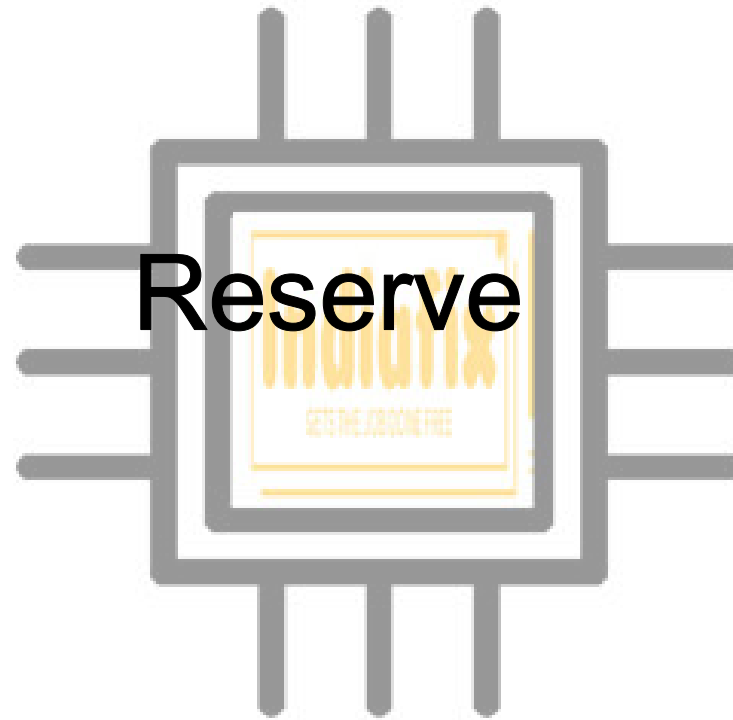


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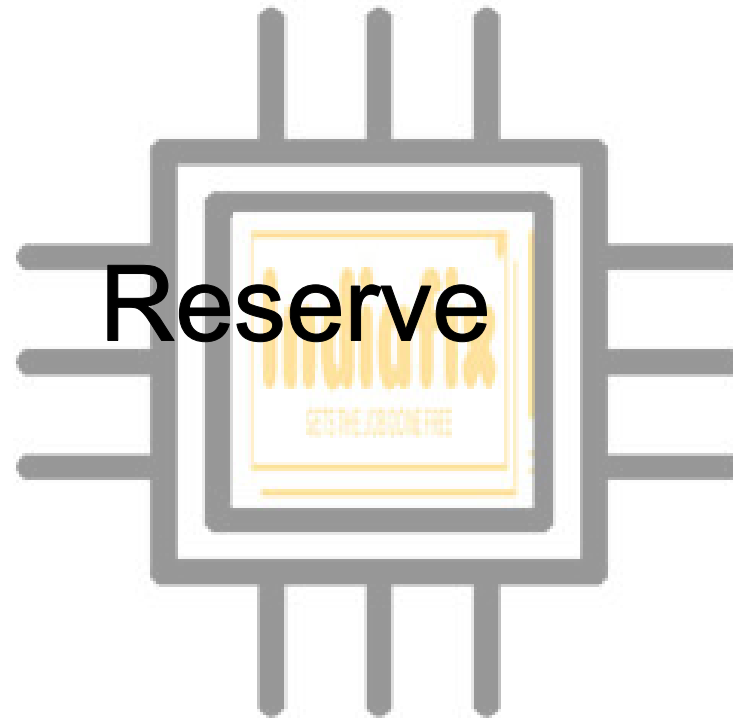
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Issued Date		2021/06/01	Deciphered Date	2027/01/01	Title
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		Size	Document Number	LA-N411P	0.1
		Date:	Thursday, December 14, 2023	Sheet	43 of 150



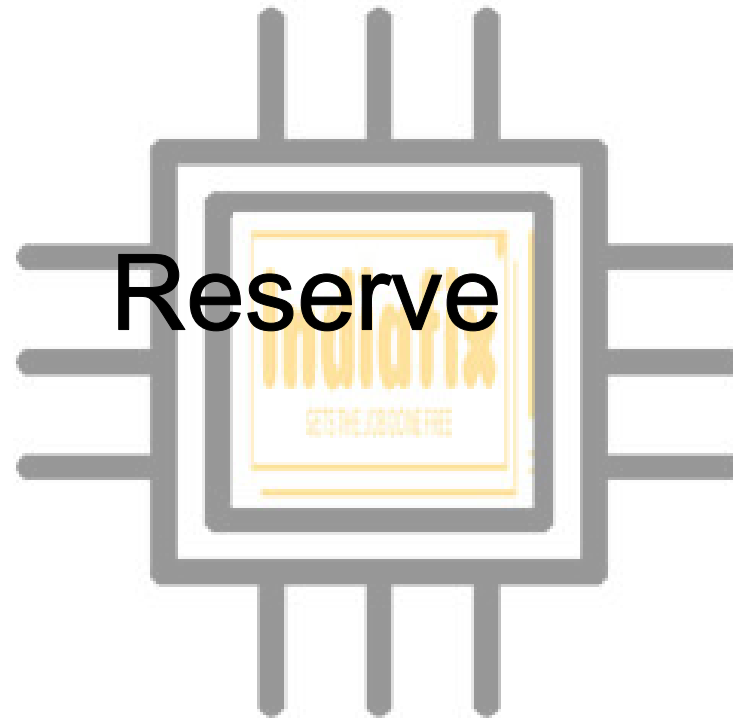
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Issued Date	2021/06/01	Deciphered Date	2027/01/01	Title	DGPU
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				Date:	Thursday, December 14, 2023
				Sheet	44 of 150



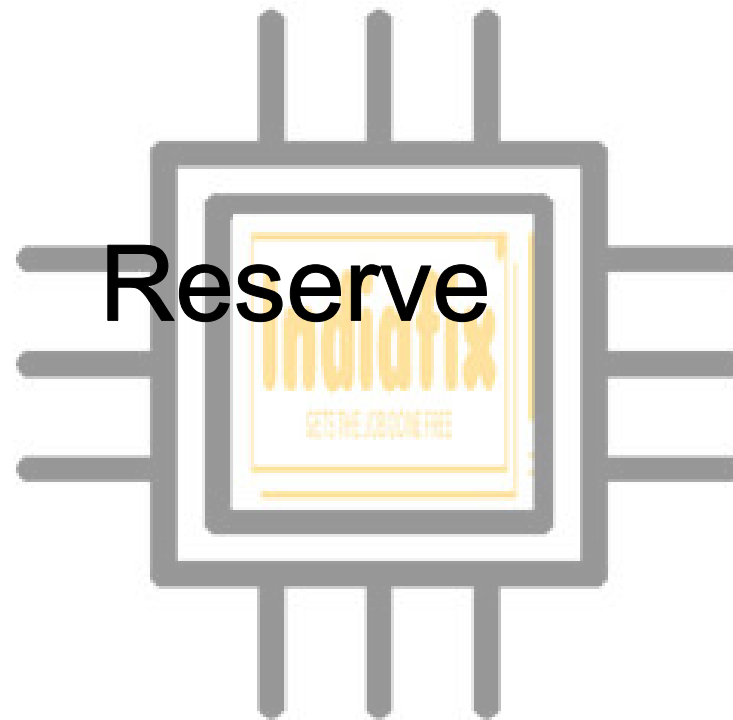
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		LA-N411P			0.1
Date:		Thursday, December 14, 2023	Sheet	45	of 150



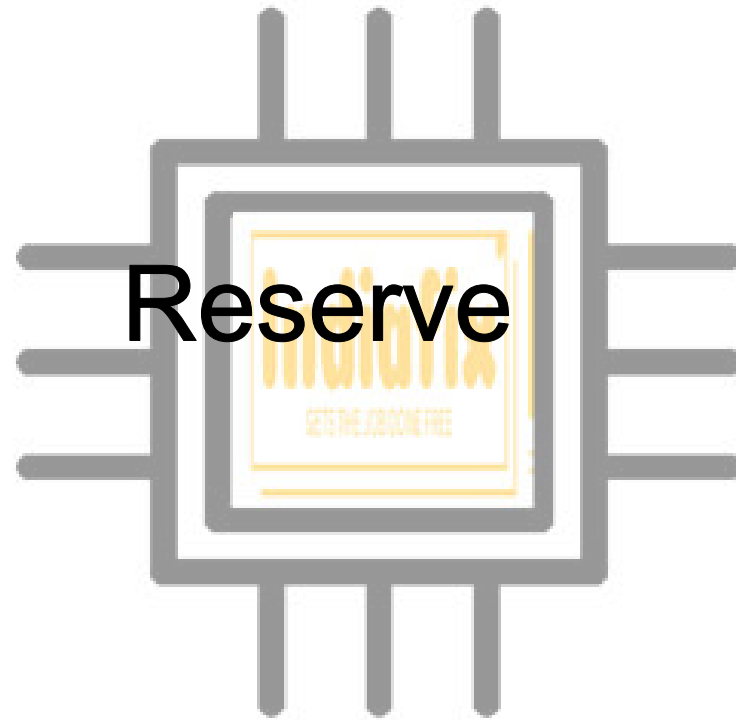
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Issued Date	2021/06/01	Deciphered Date	2027/01/01	Title	DGPU
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				Date:	Thursday, December 14, 2023
				Sheet	46 of 150



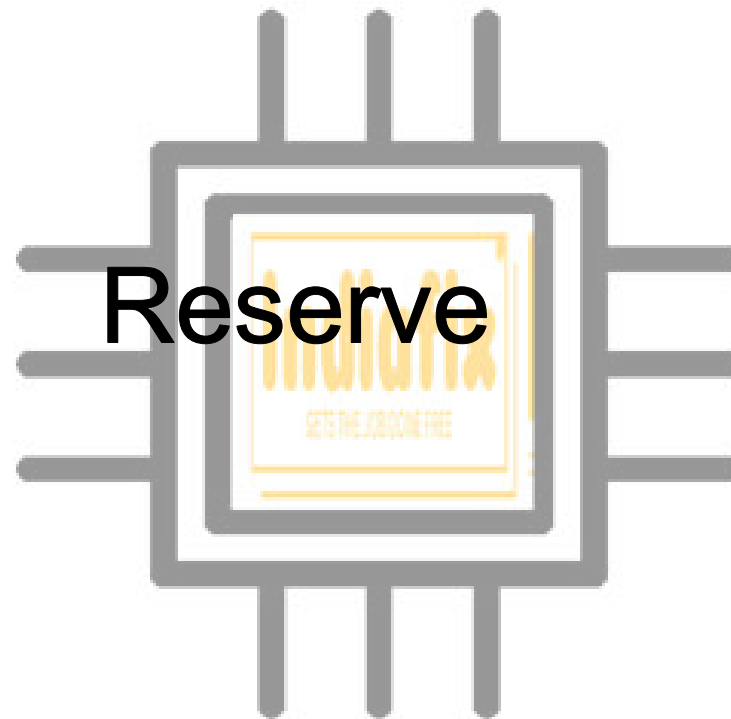
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				Date:	Thursday, December 14, 2023
				Sheet	47 of 150



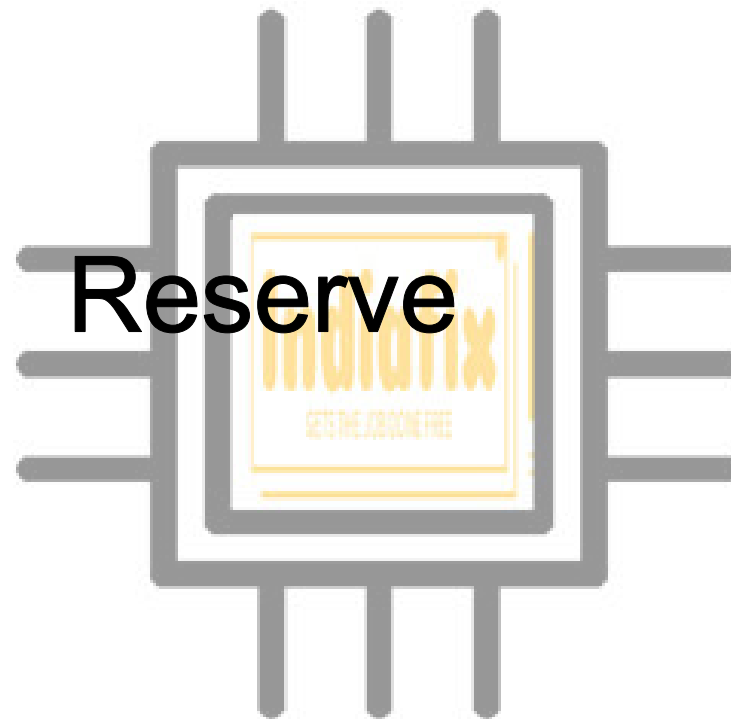
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		Size	Document Number		Rev
		B	LA-N411P		0.1
Date:		Thursday, December 14, 2023		Sheet	48 of 150



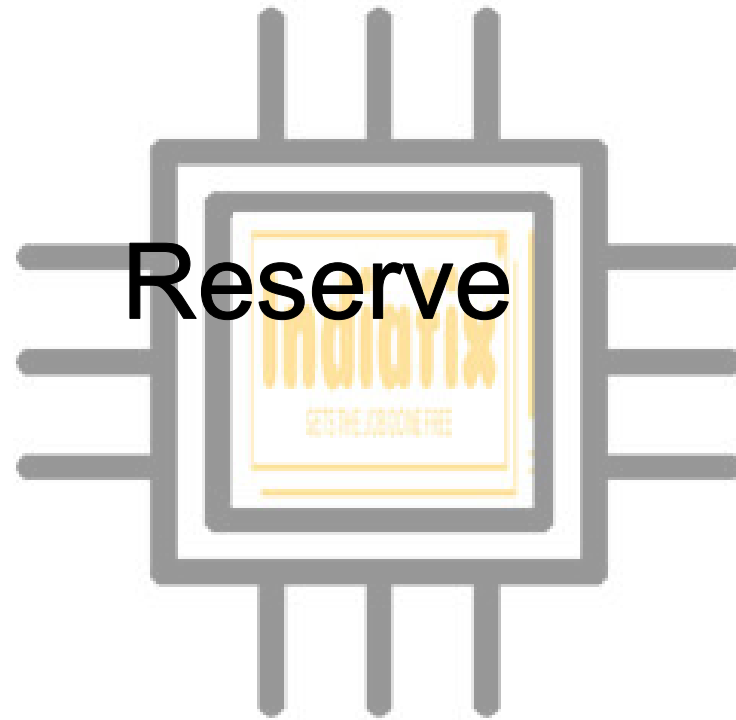
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Issued Date	2021/06/01	Deciphered Date	2027/01/01	Title	VRAM	
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				Date:	Thursday, December 14, 2023	Sheet 49 of 150



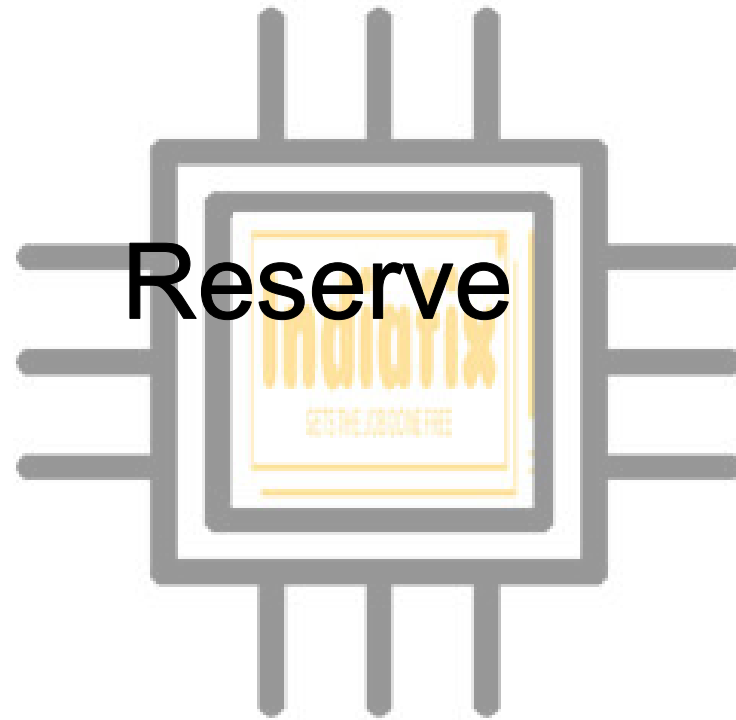
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Issued Date	2021/06/01	Deciphered Date	2027/01/01	Title VRAM		
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				Date:	Thursday, December 14, 2023	Sheet 50 of 150



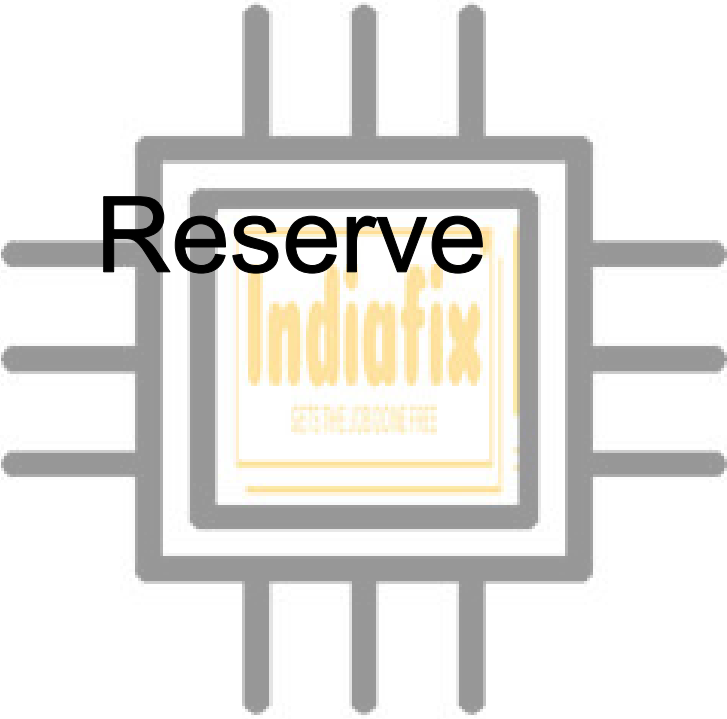
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				B	LA-N411P	0.1
				Date:	Thursday, December 14, 2023	Sheet 51 of 150



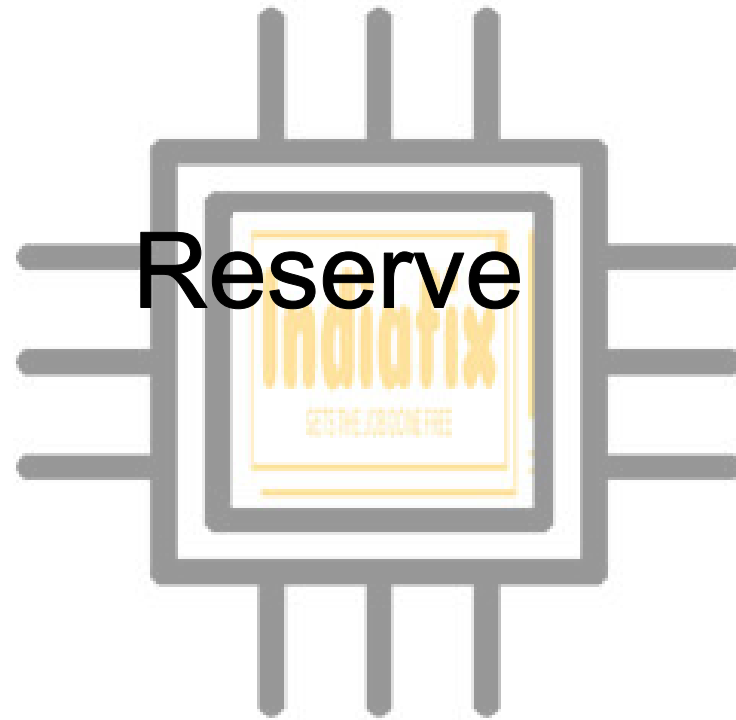
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				Date: Thursday, December 14, 2023	Sheet 53 of 150

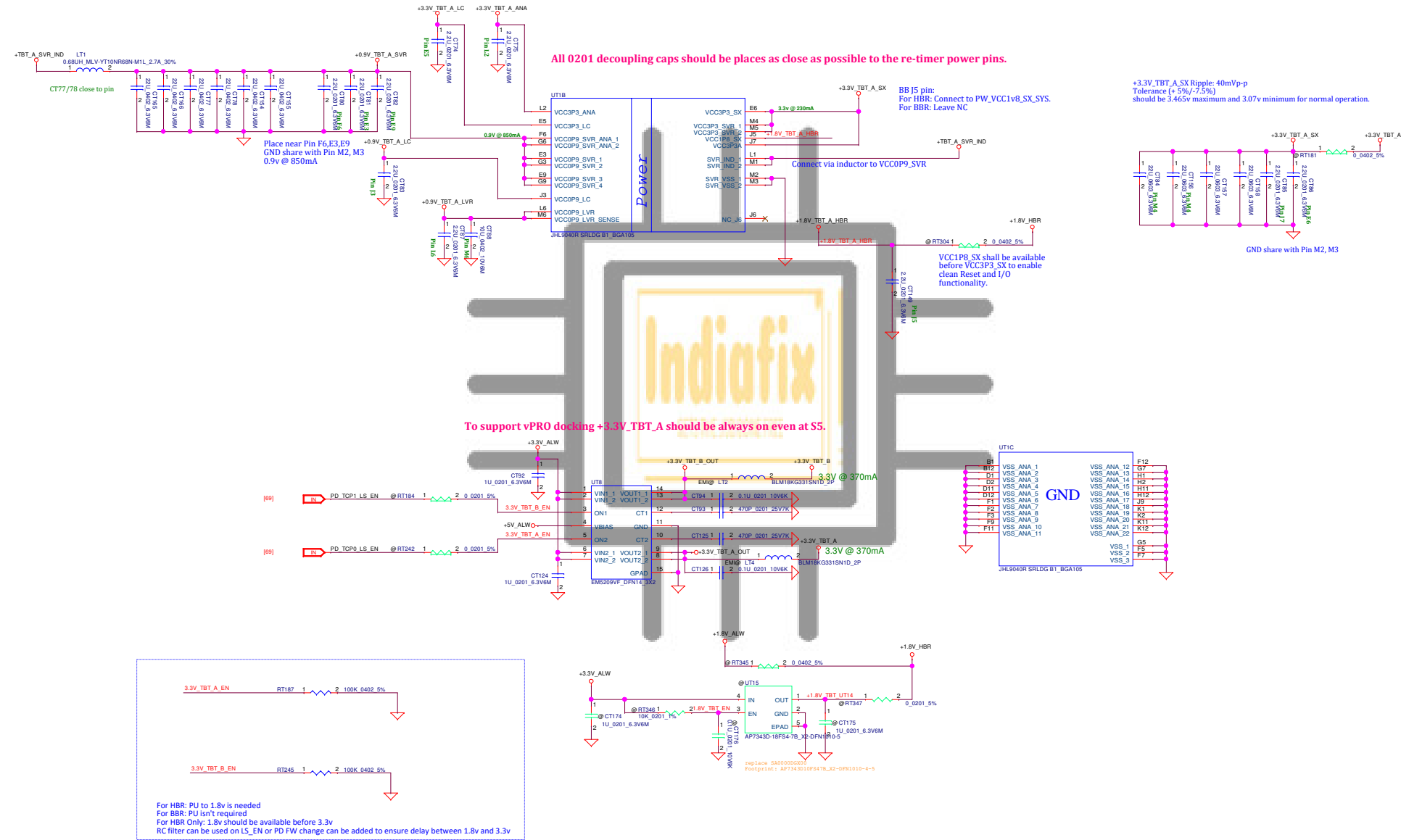


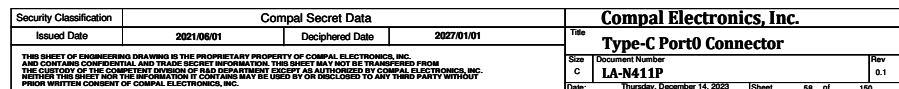
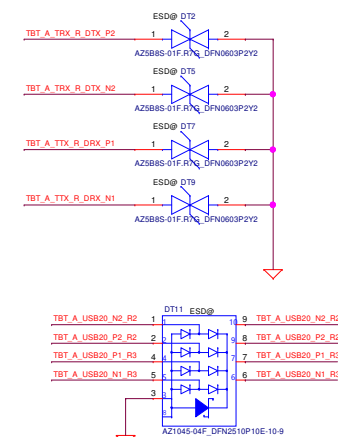
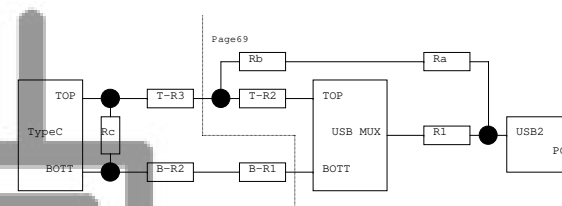
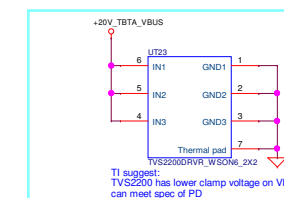
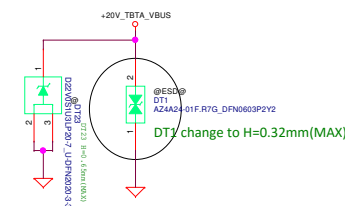
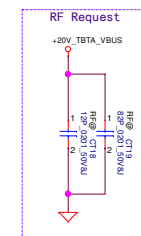
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				Date:	Thursday, December 14, 2023	Sheet 54 of 150

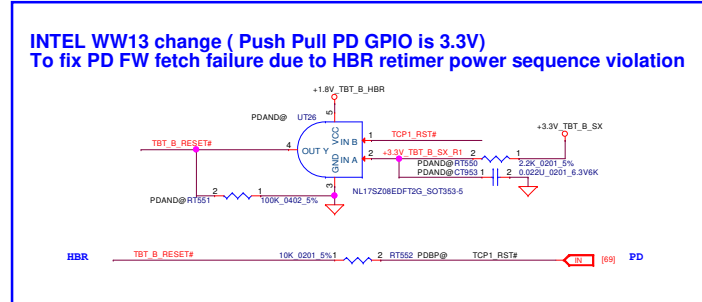
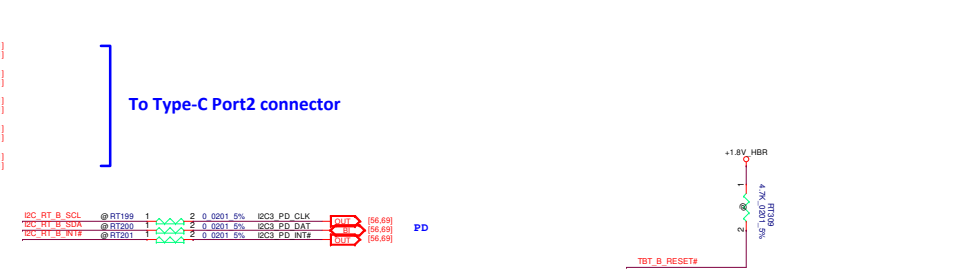


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		Size	Document Number	LA-N411P	0.1
		Date:	Thursday, December 14, 2023	Sheet	55 of 150

Manufacture	P/N	Value [uH]	Max Rdc [mΩ]	Isat [A]	Dimensions
Murata	DfE201610E-R68M=P2	0.68	43	4.3	2.0 x 1.6 x 1.0 mm
Murata	DfE201612E-R68M=P2	0.68	33	4.8	2.0 x 1.6 x 1.2 mm
Vishay	IHLp1212ABERR68M11	0.68	25	5.5	3.0 x 3.65 x 1.2 mm







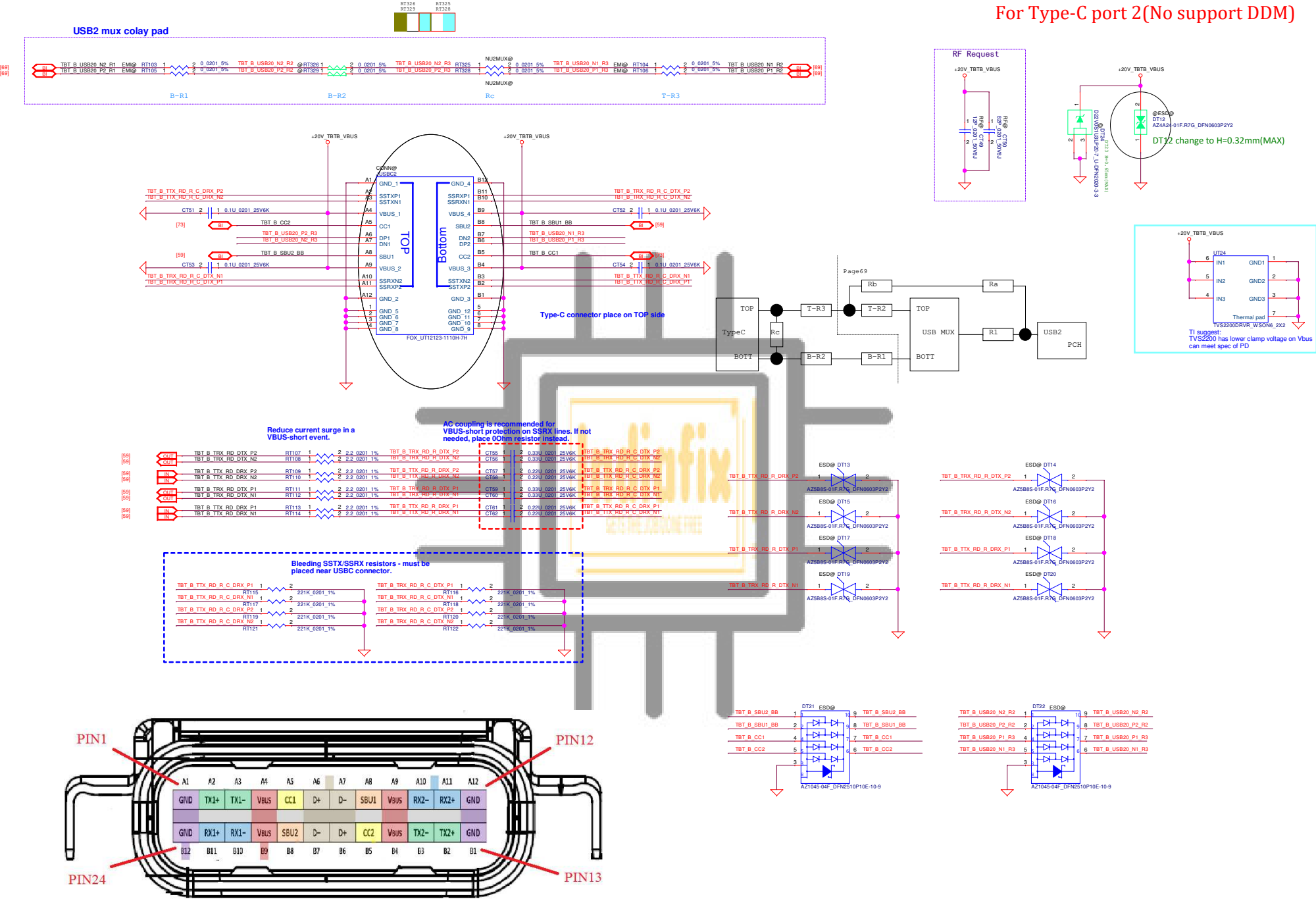
Straps

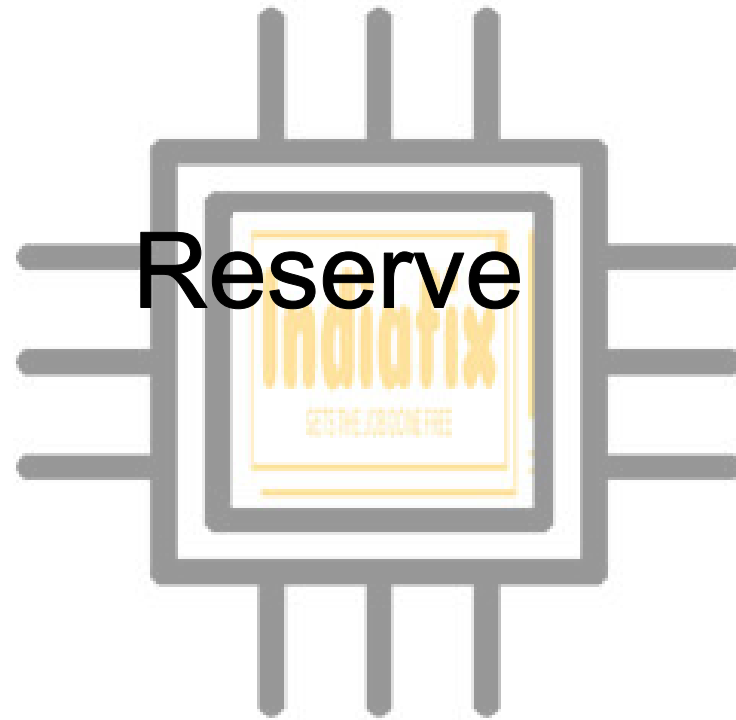


Figure 10. BBR-A0 PLL Issue Workaround reserved

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					LA-N411P	0.1
				Date	Thursday, December 14, 2023	Sheet 59 of 150

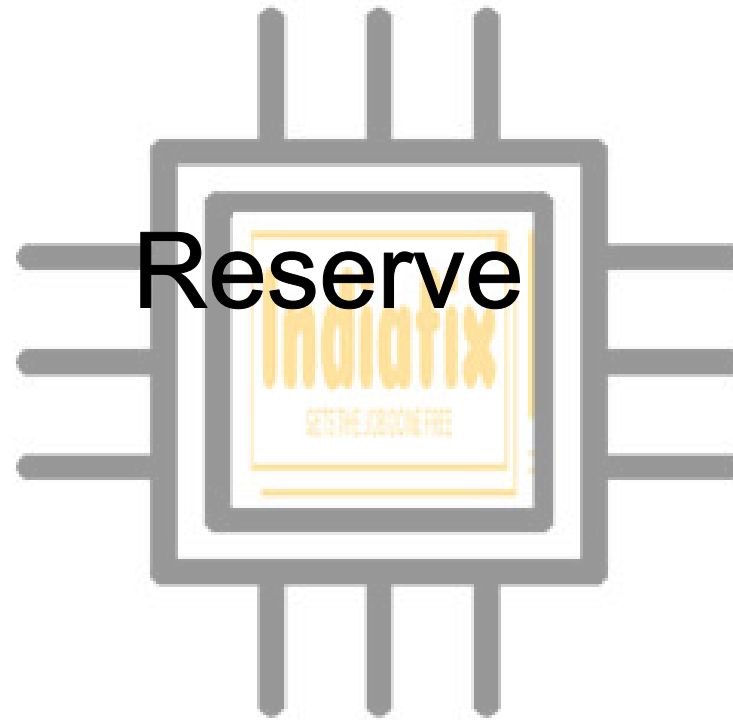
For Type-C port 2(No support DDM)





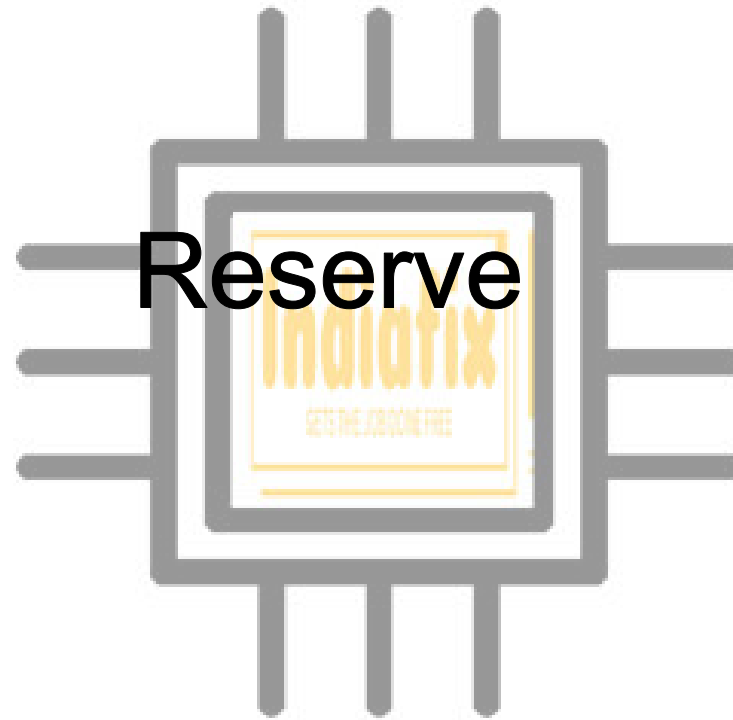
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		Size	Document Number	LA-N411P	0.1
		Date:	Thursday, December 14, 2023	Sheet	62 of 150

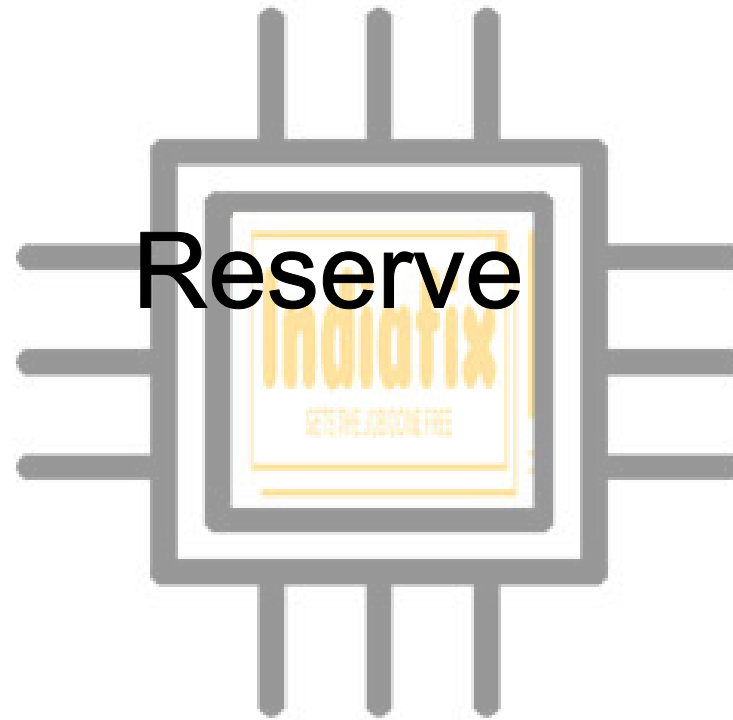


Reserve

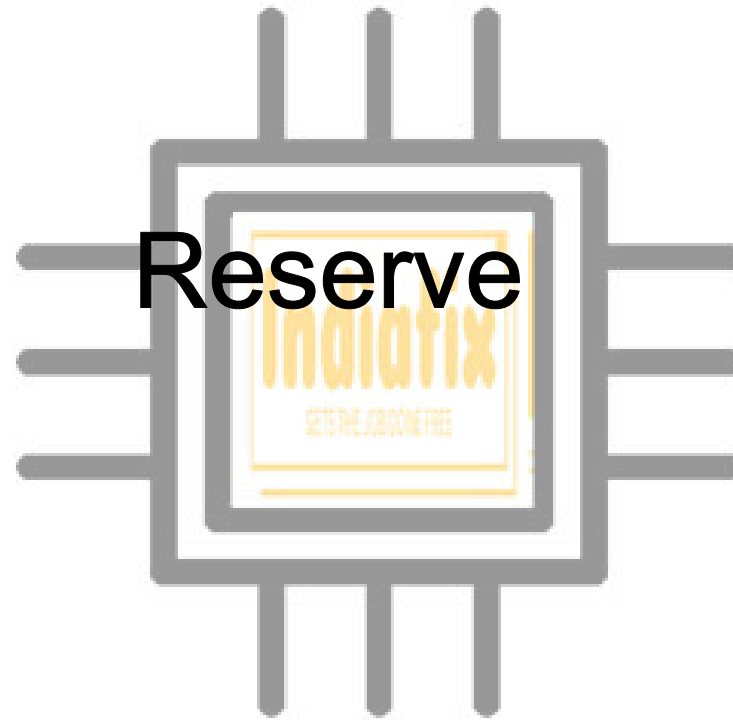
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Issued Date	2021/06/01	Deciphered Date	2027/01/01	Title	Type-C Port2 Re-Timer	
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				B	LA-N411P	0.1
				Date:	Thursday, December 14, 2023	Sheet 63 of 150



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Issued Date	2021/06/01	Deciphered Date	2027/01/01	Title	Type-C Port2 Connector	
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				B	LA-N411P	0.1
				Date:	Thursday, December 14, 2023	Sheet 64 of 150

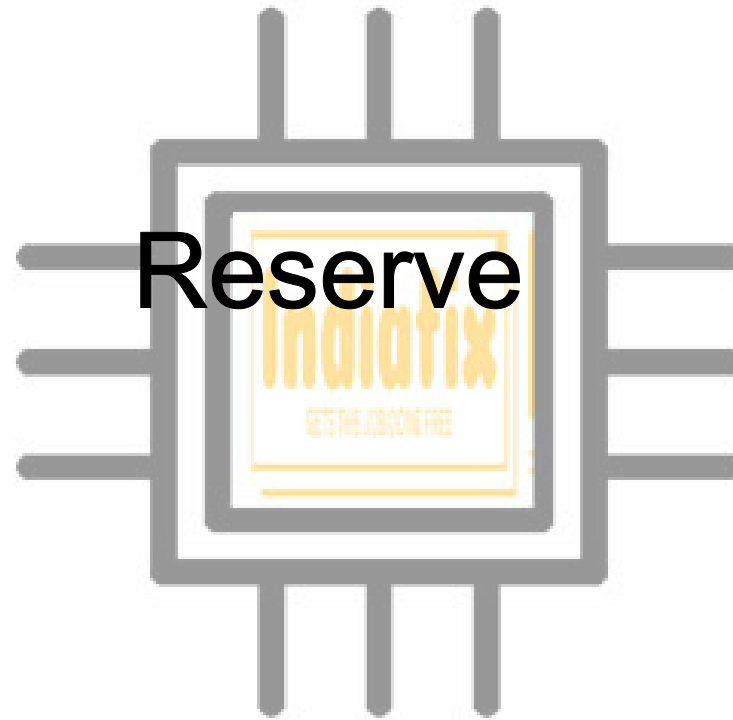


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		Size	Document Number	Rev	
		B	LA-N411P	0.1	
Date:		Thursday, December 14, 2023	Sheet	65	of 150

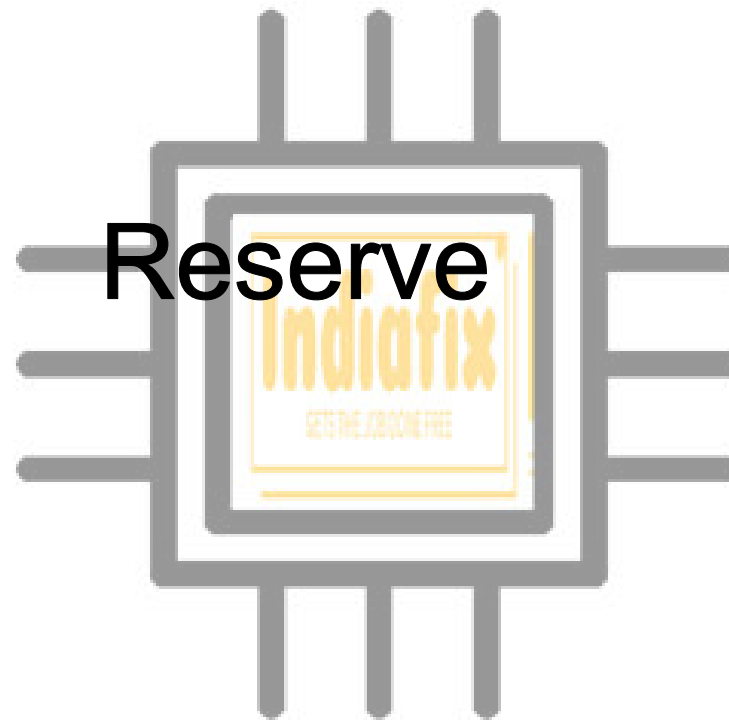


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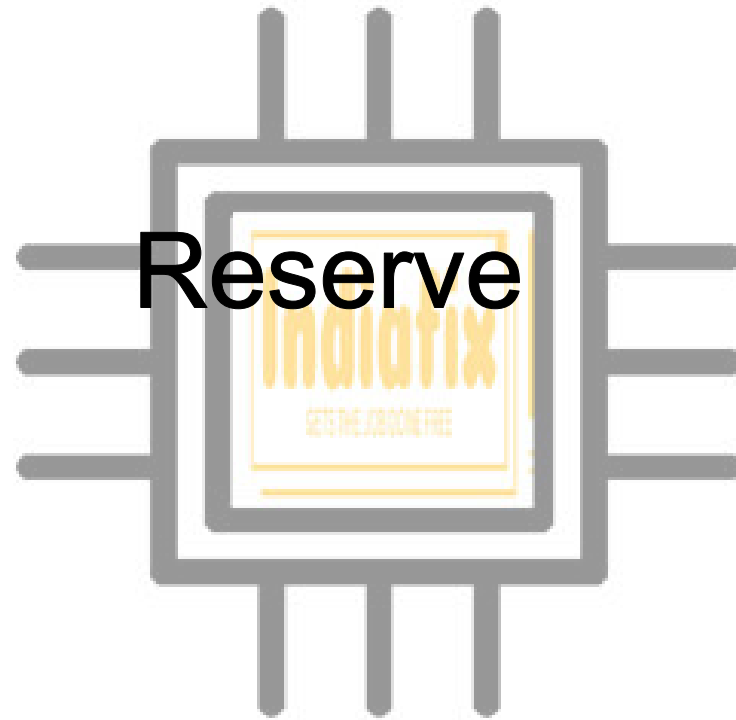
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Issued Date	2021/06/01	Deciphered Date	2027/01/01	Title	Type-C Port3 Re-Timer	
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				B	LA-N411P	0.1
				Date:	Thursday, December 14, 2023	Sheet 66 of 150



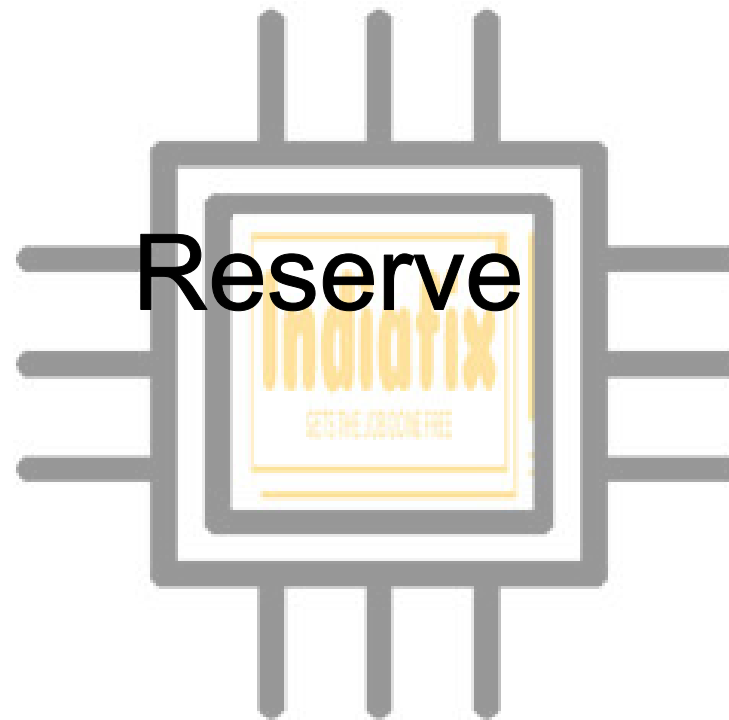
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Issued Date	2021/06/01	Deciphered Date	2027/01/01	Title		
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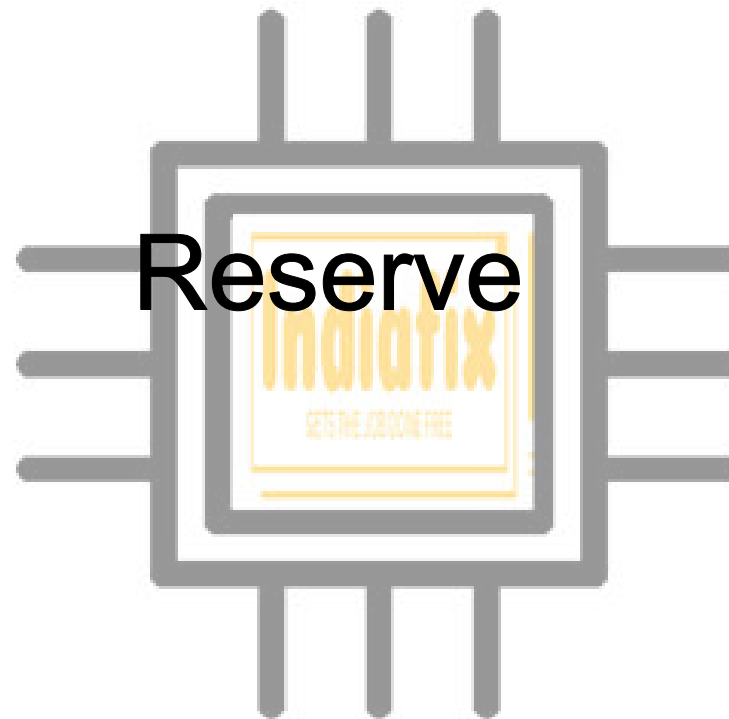
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Issued Date	2021/06/01	Deciphered Date	2027/01/01	Title	
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				Date: Thursday, December 14, 2023	Sheet 70	of 150



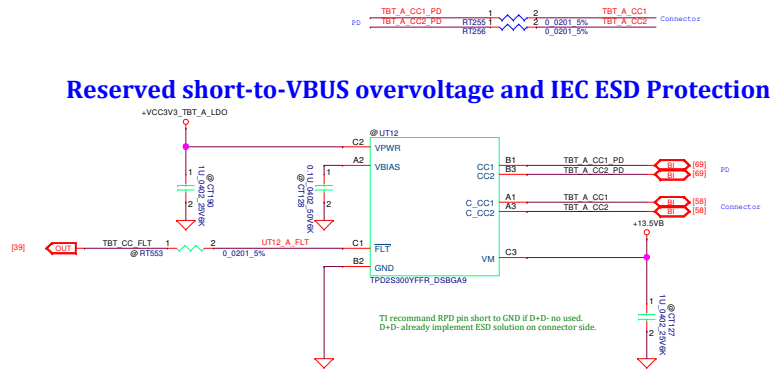
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Issued Date	2021/06/01	Deciphered Date	2027/01/01	Title PD Controller		
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				Date:	Thursday, December 14, 2023	Sheet 71 of 150



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				Date: Thursday, December 14, 2023	Sheet 72 of 150

Type-C Port 1

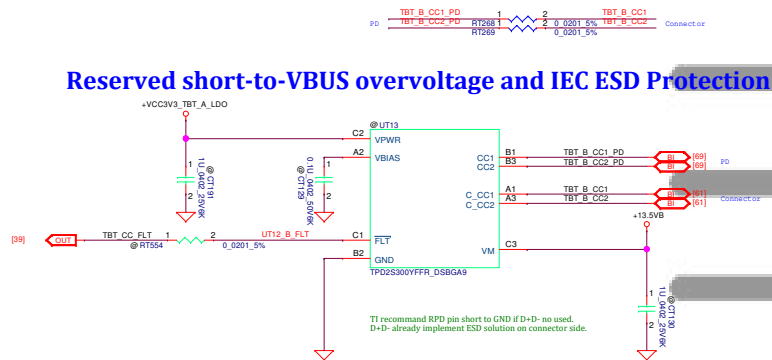
Support CCD Bypass



Reserved short-to-VBUS overvoltage and IEC ESD Protection

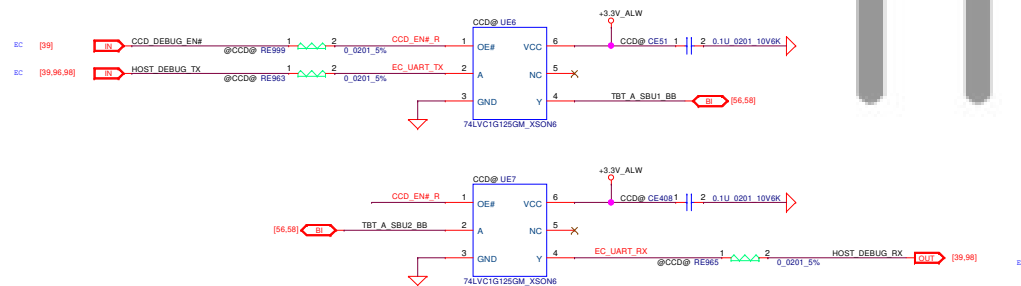
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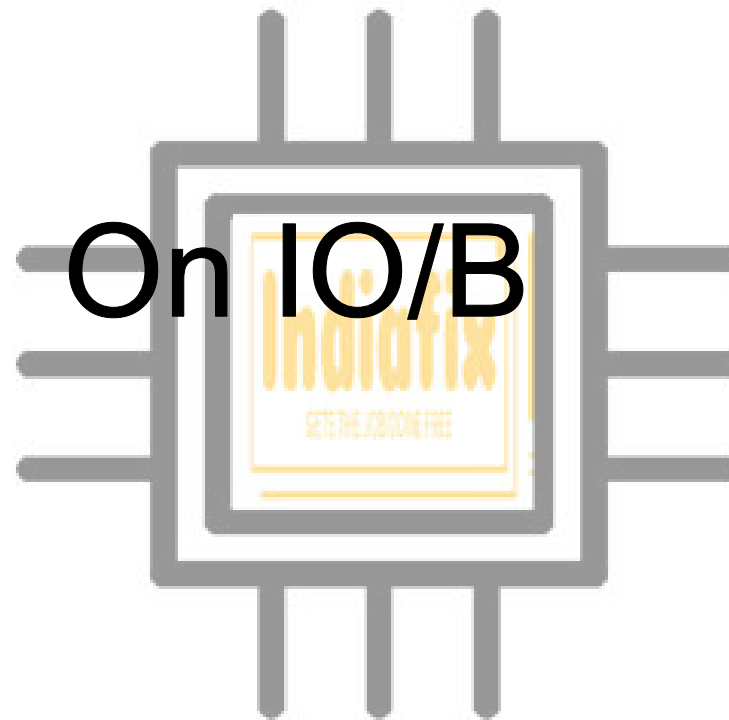
Bypass



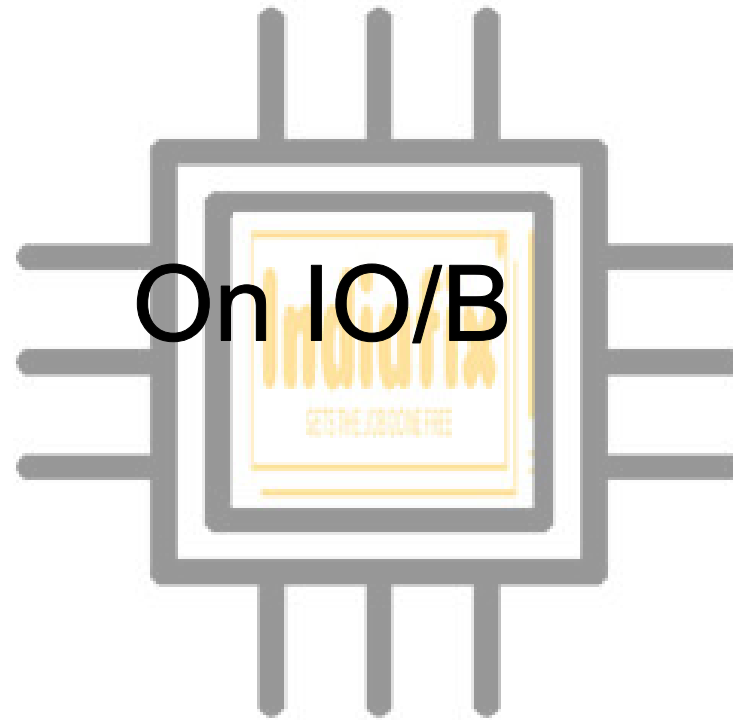
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Support Close Chassis Debug (CCD)

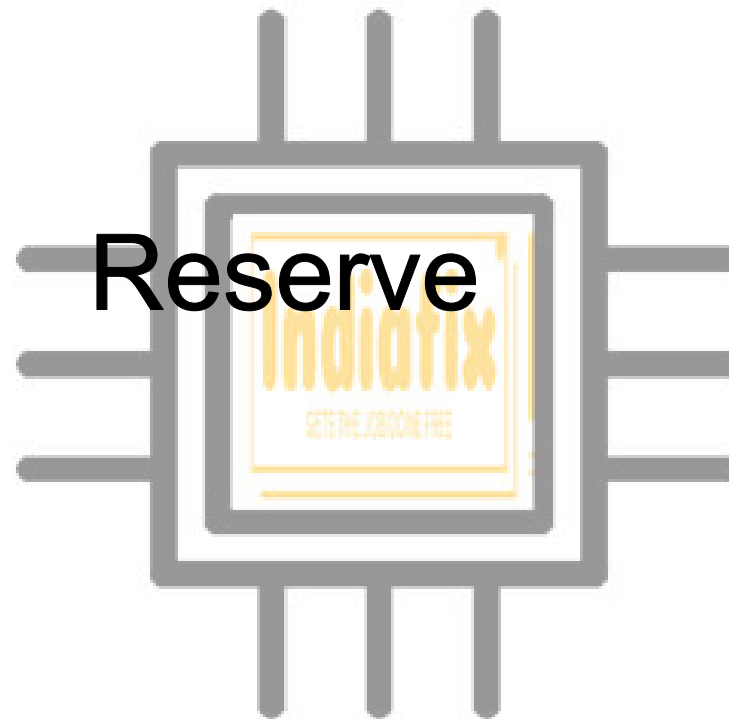




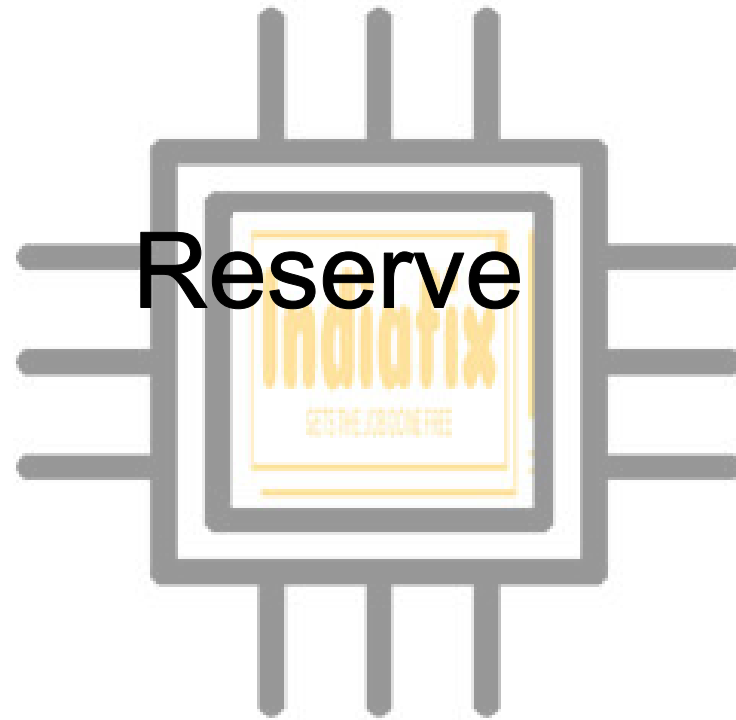
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		Size	Document Number		Rev	
		A	LA-N411P		0.1	
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					Document Number
		LA-N411P			Rev
		Date: Thursday, December 14, 2023			0.1
		Sheet 75 of 150			

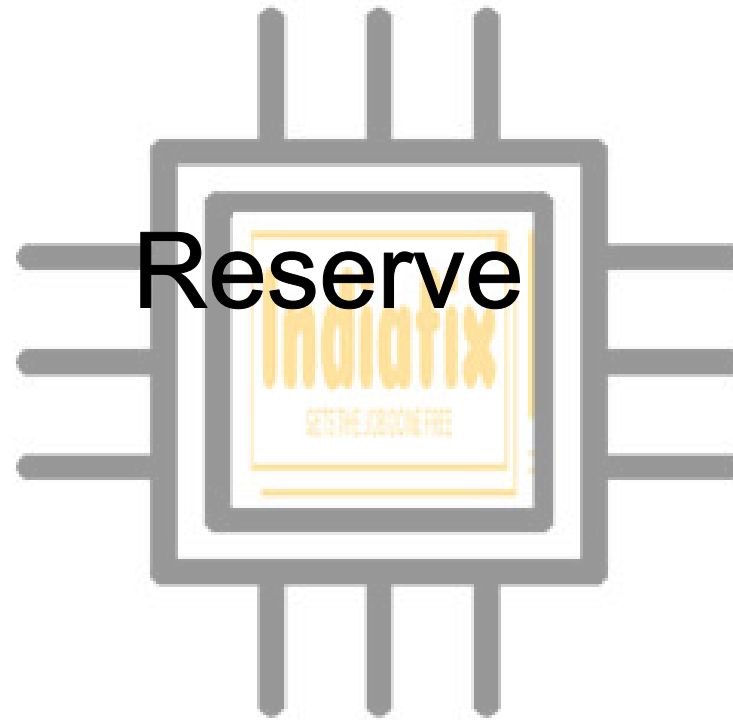


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		Size B	Document Number LA-N411P	Rev 0.1	Date: Thursday, December 14, 2023
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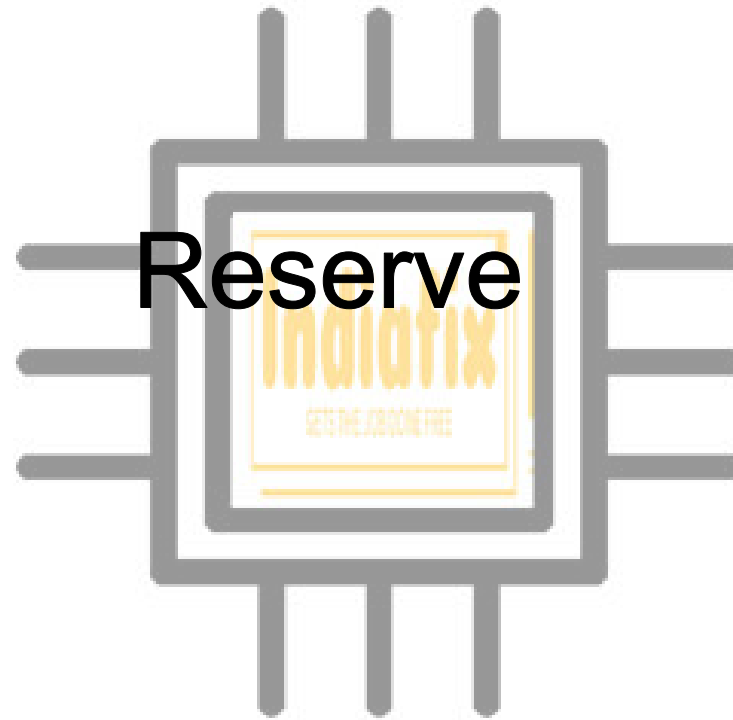
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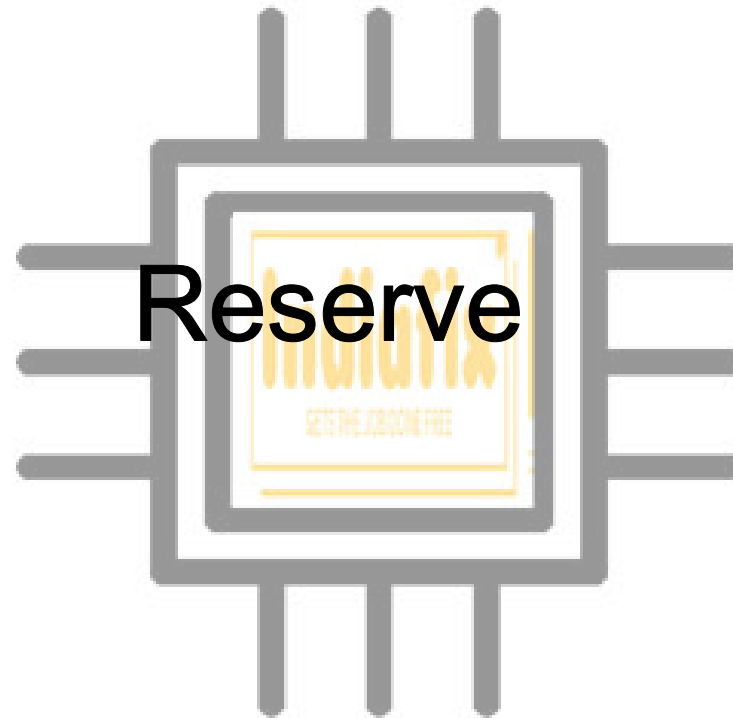
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		Size	Document Number	Rev	
		B	LA-N411P	0.1	
Date:		Thursday, December 14, 2023	Sheet	78 of 150	

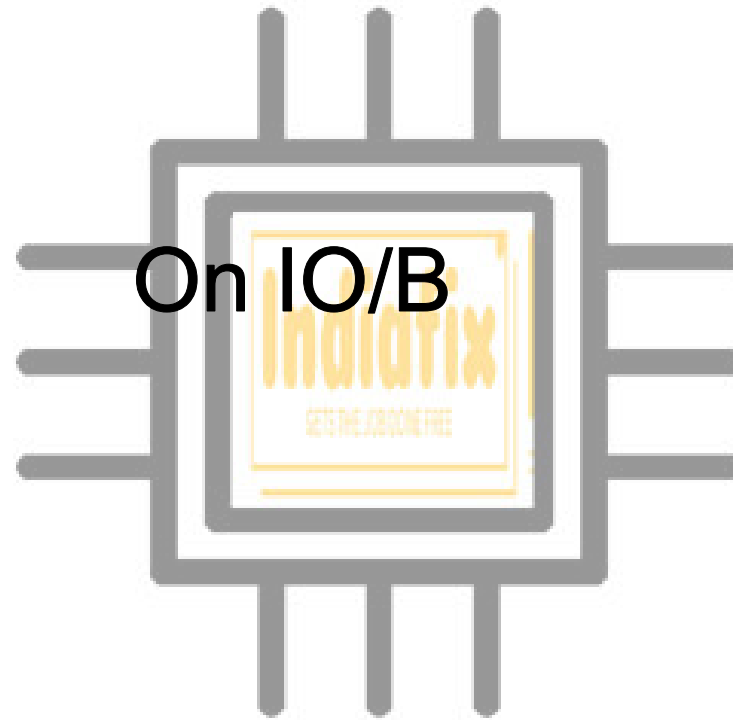


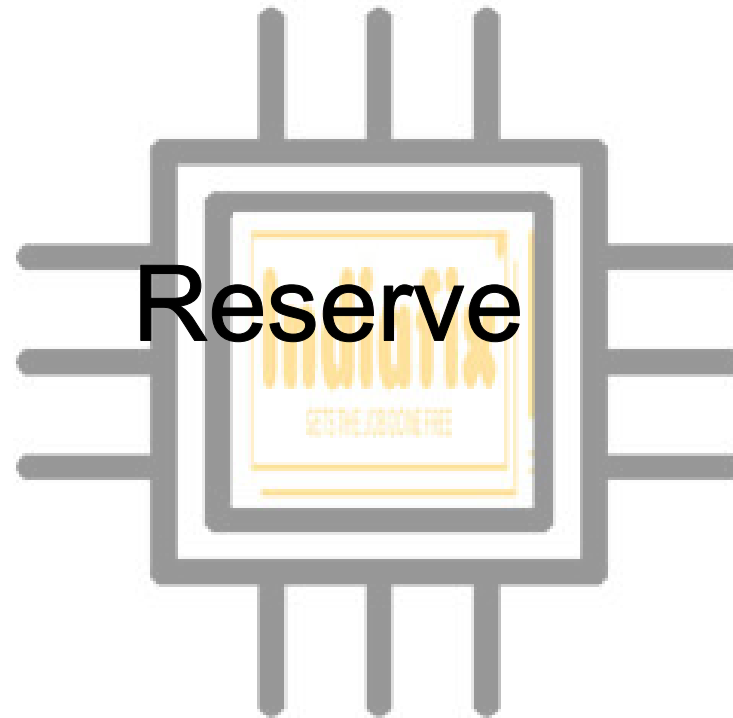
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		Size	Document Number	Rev	
		B	LA-N411P	0.1	
		Date:	Thursday, December 14, 2023	Sheet	79 of 150

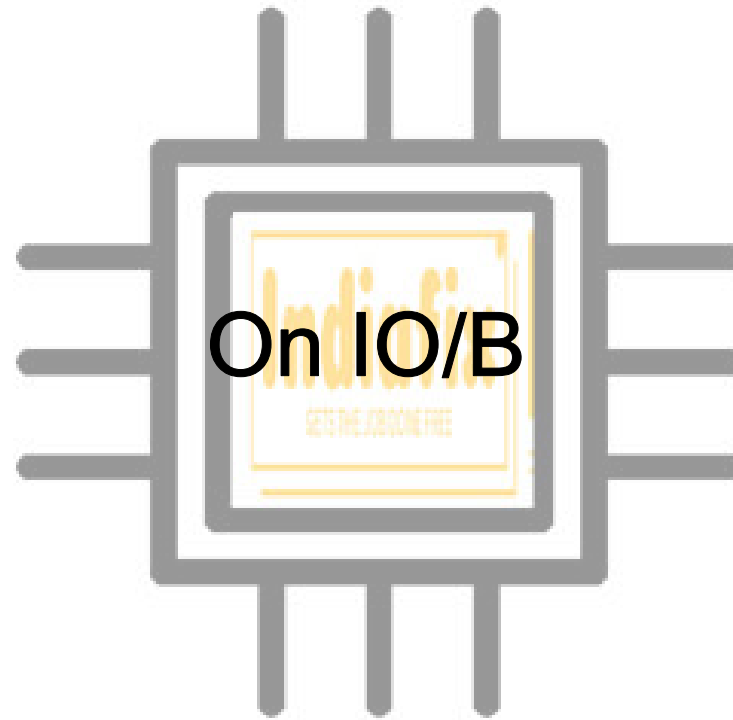


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				Sheet	80 of 150

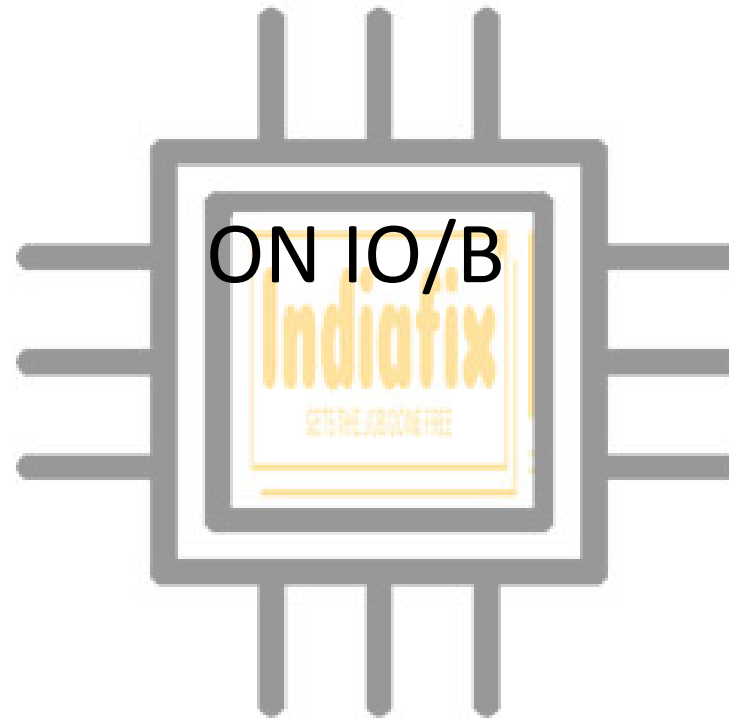


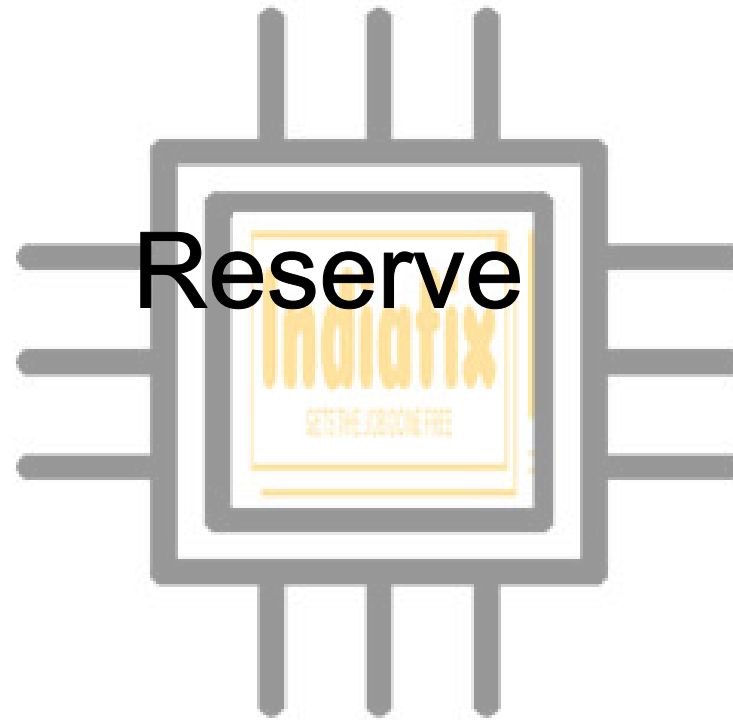


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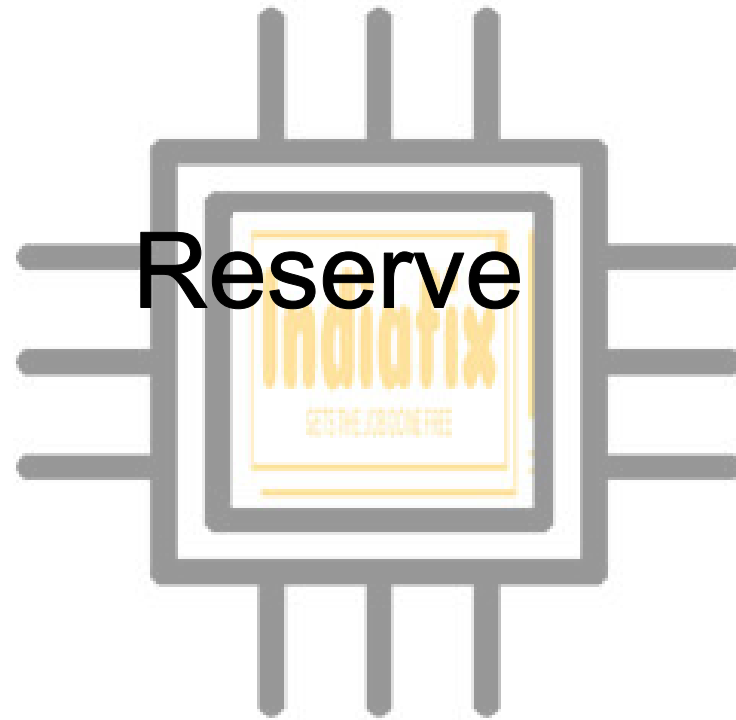


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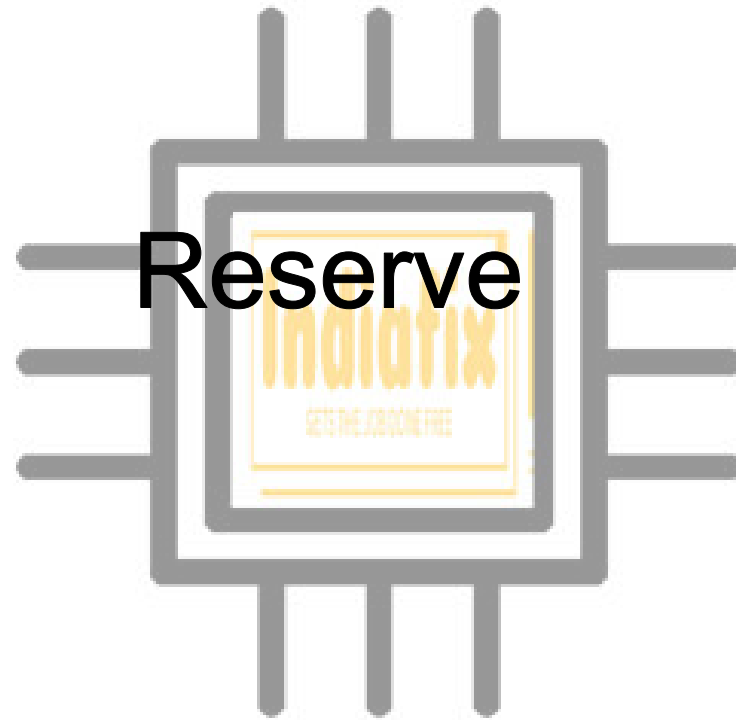
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Compal Electronics, Inc.
Amplifier & Speaker Conn.

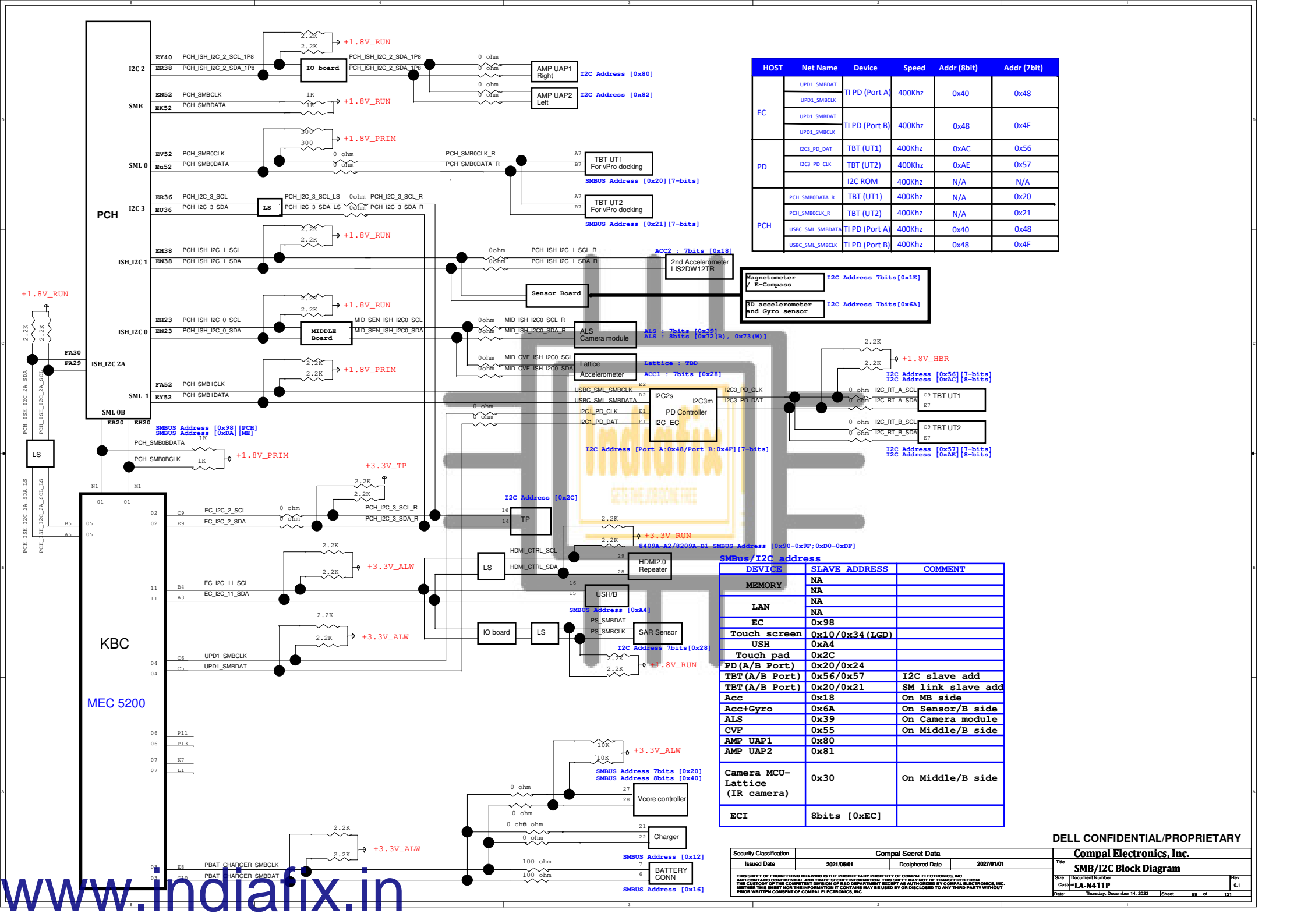
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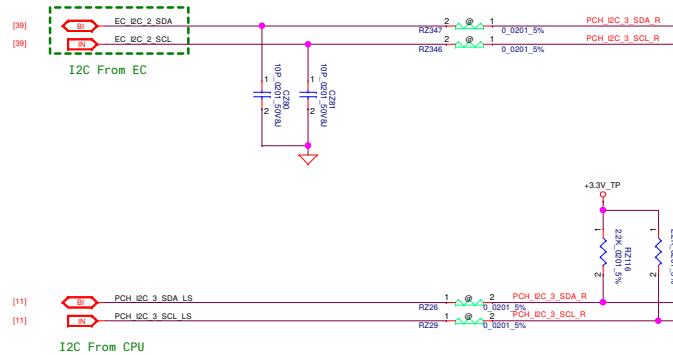
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		Size B	Document Number LA-N411P	Rev 0.1	Date: Thursday, December 14, 2023
		Sheet		88	of 150

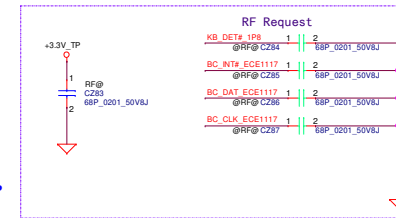
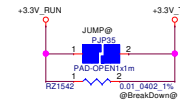


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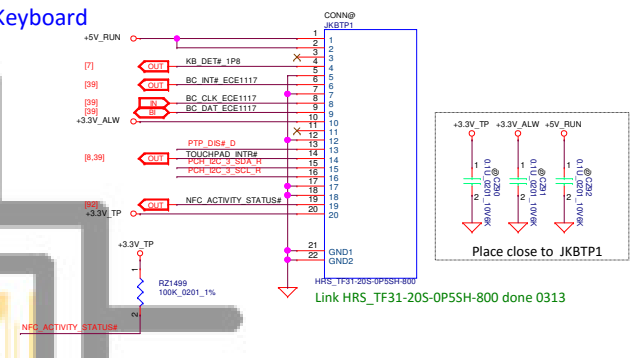


Plan is for I2C to be driven by the EC for Win7 and Pre-OS (will utilize Intel I2C drivers for Win7)
For Win8.1 and 10 the EC will control TP over I2C Pre-OS and then the PCH will drive I2C when in Windows
Route PS2 from EC to the touch pad also for contingency plan if EC has issues

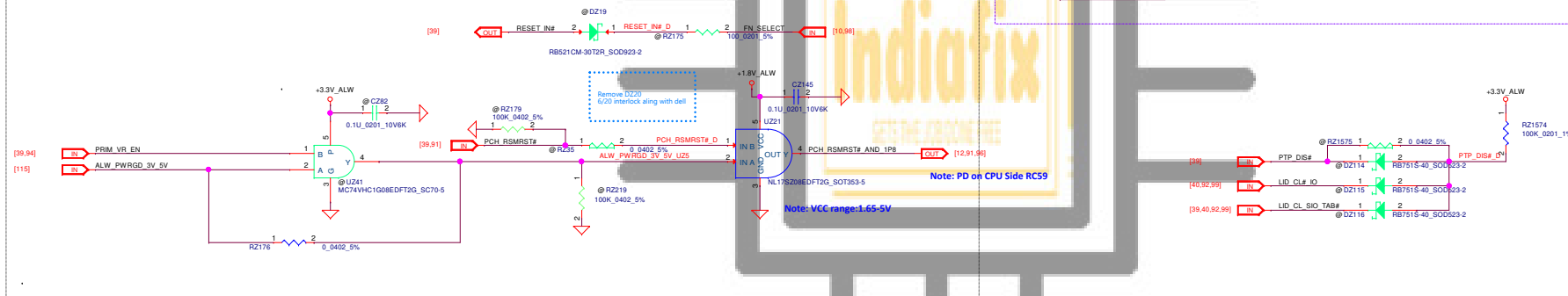
RZ1542 Need to change depop before MP



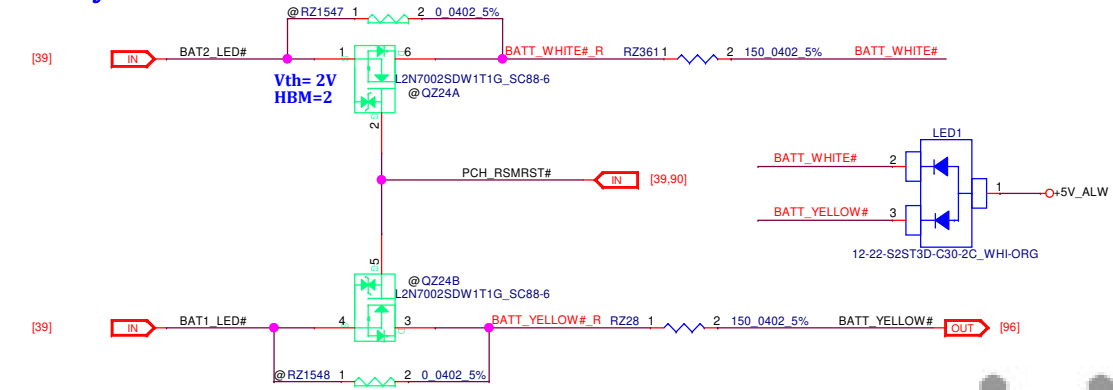
Keyboard



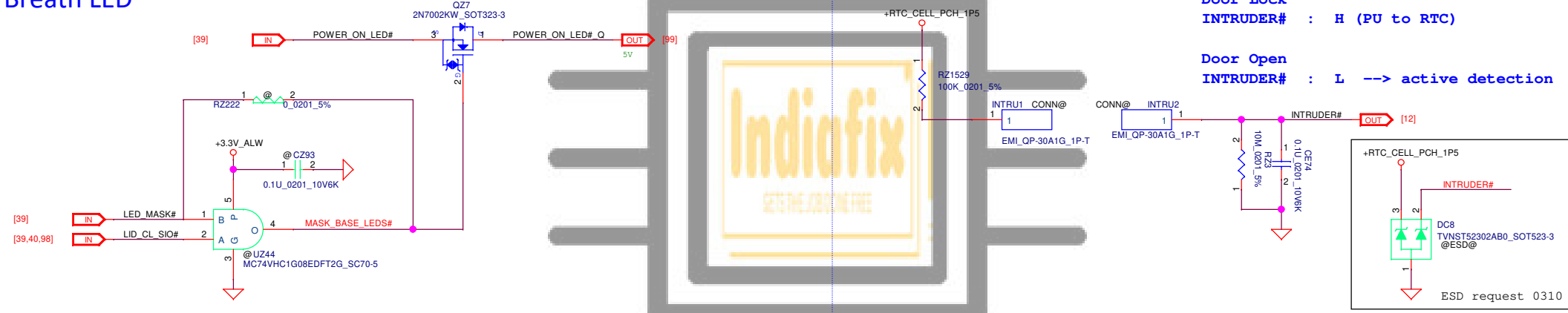
RSMRST circuit



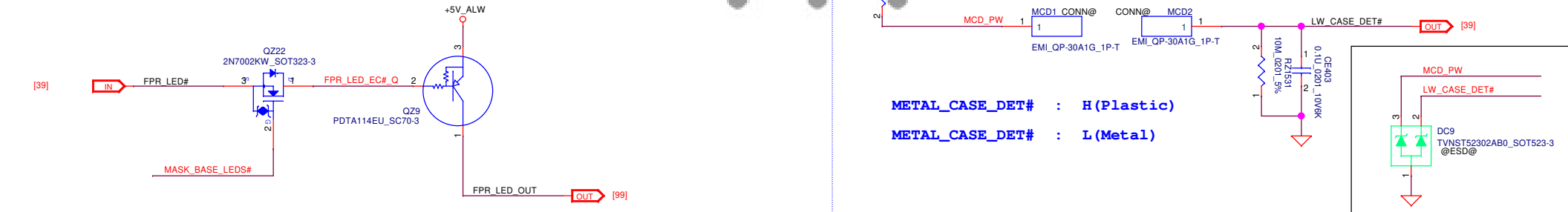
Battery LED



Breath LED

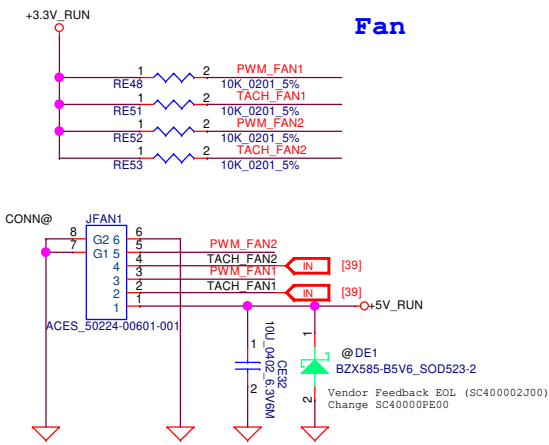


02/20 got the message update for LED * 4pcs inside FPR



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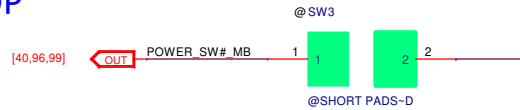
Fan



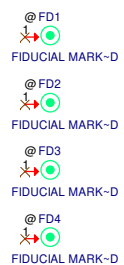
TBT BBR Crystal Shielding Can

Gasket

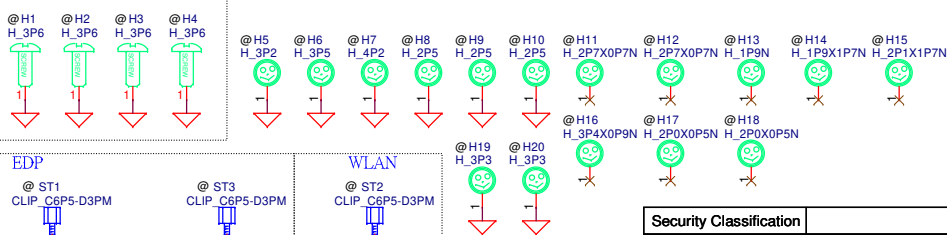
POWER & INSTANT ON SWITCH TOP



Fiducial Mark



CPU



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+3.3V_PRIM

Ray0325: follow RVP 0.7 page207
support INTERPOSER pop R2105, depop R2237

+1.8V_PRIM

+3.3V_WWAN source

ON IO/B

+5V_RUN source

RZ1546 Need to change depop before MP

+3.3V_WLAN/+1.8V_RUN source

RZ1540 Need to change depop before MP

+3.3V_RUN source

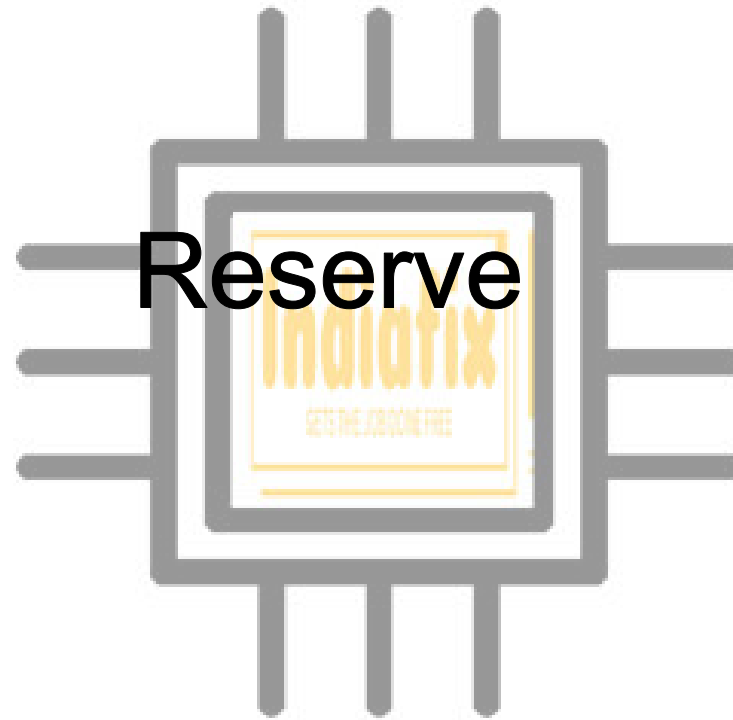
RZ1543 Need to change depop before MP

EC request to reserve OR gate for WLAN power enable

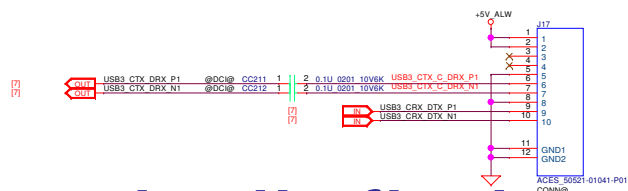
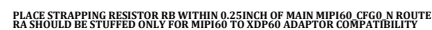
CZ406-CZ408 Close PJP503

CZ406-CZ408 add
by RF Zarco

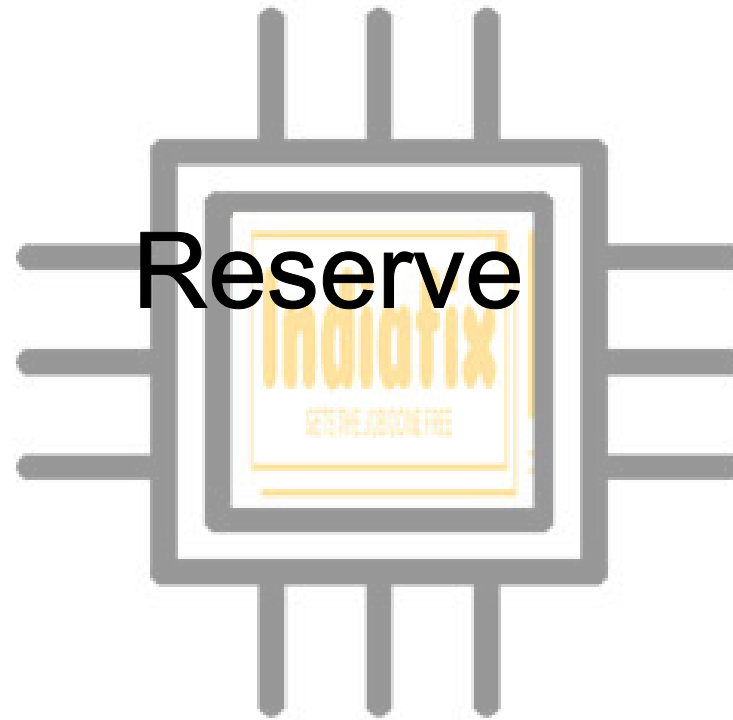
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		Size B	Document Number LA-N411P	Rev 0.1	Date: Thursday, December 14, 2023 Sheet 95 of 150

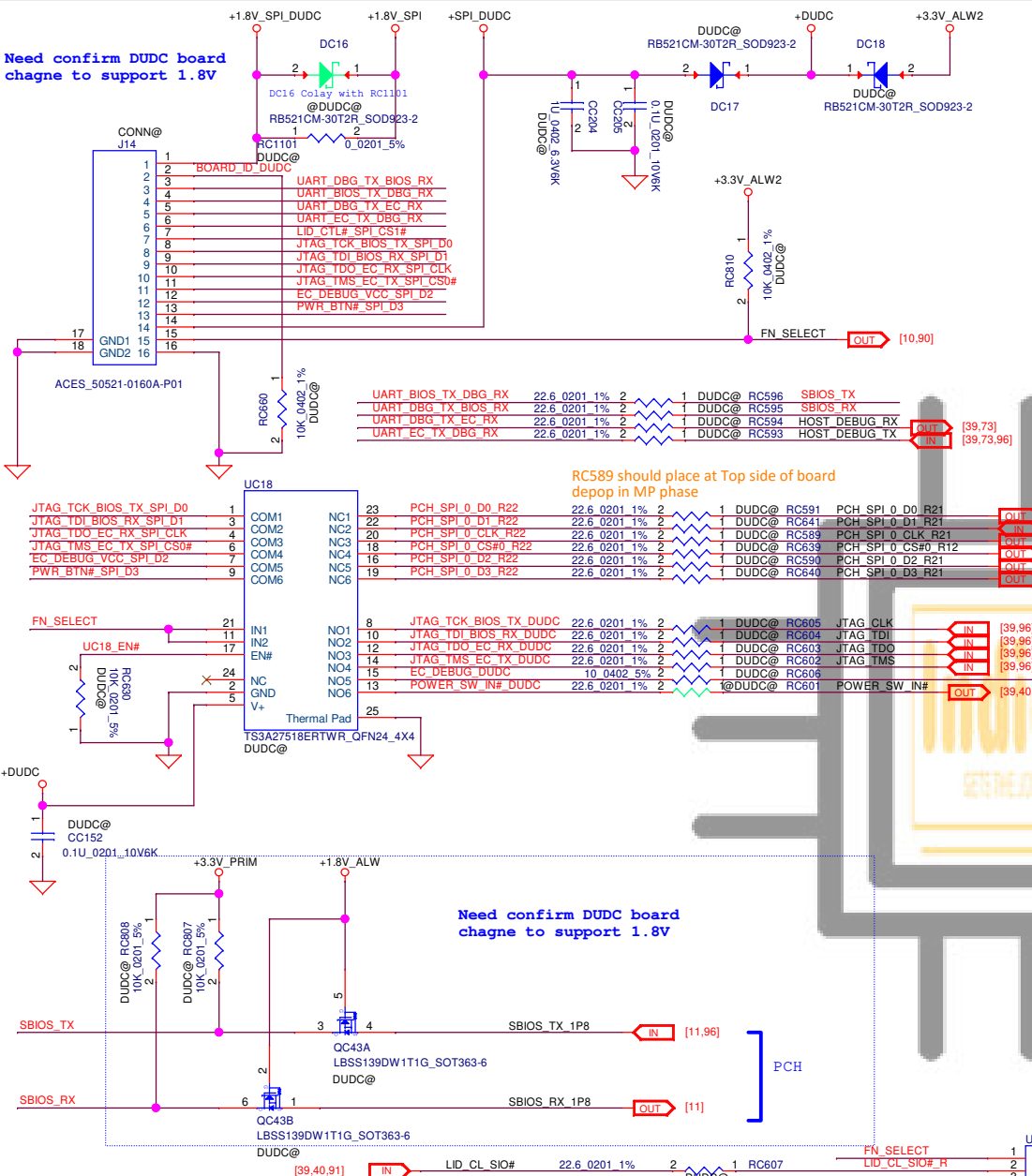


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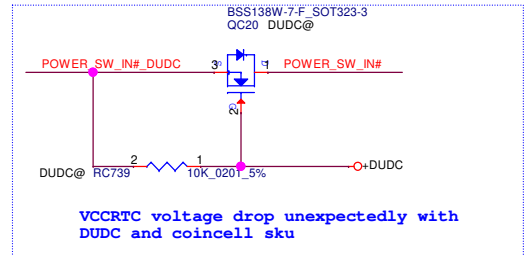
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Need confirm DUDC board chagne to support 1.8V



For DUDC debug
DUDC Gen2 Function Table

Pin	Pin Name	Function0 (SPI)	Function1 (Debug)
1	+1.8V_SPI_DUDC	+1.8V_SPI_DUDC	+1.8V_SPI_DUDC
2	BOARD_ID_DUDC	BOARD_ID_DUDC	BOARD_ID_DUDC
3	UART_DBG_TX_BIOS_RX	SBIOS_RX_1P8	SBIOS_RX_1P8
4	UART_BIOS_TX_DBG_RX	SBIOS_TX_1P8	SBIOS_TX_1P8
5	UART_DBG_TX_EC_RX	HOST_DEBUG_RX	HOST_DEBUG_RX
6	UART_EC_TX_DBG_RX	HOST_DEBUG_TX	HOST_DEBUG_TX
7	LID_CTL#_SPI_CS1#	NA	LID_CL_SIO#
8	JTAG_TCK_BIOS_TX_SPI_D0	SHD_IO0	JTAG_CLK
9	JTAG_TDI_BIOS_RX_SPI_D1	SHD_IO1	JTAG_TDI
10	JTAG_TDO_EC_RX_SPI_CLK	SHD_IO0	JTAG_CLK
11	JTAG_TMS_EC_TX_SPI_CS0#	SHD_CS#0	JTAG_TMS
12	EC_DEBUG_VCC_SPI_D2	SHD_IO2	EC_DEBUG_DUDC
13	PWR_BTN#_SPI_D3	SHD_IO3	POWER_SW_IN#
14	+SPI_DUDC	+SPI_DUDC	+SPI_DUDC
15	FN_SELECT	MUX_CTRL=0	MUX_CTRL=1
16	GND	GND	GND

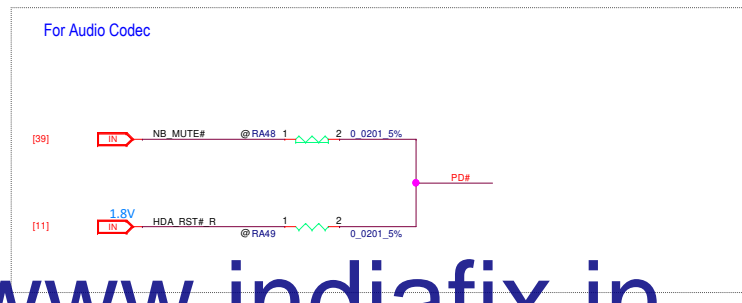
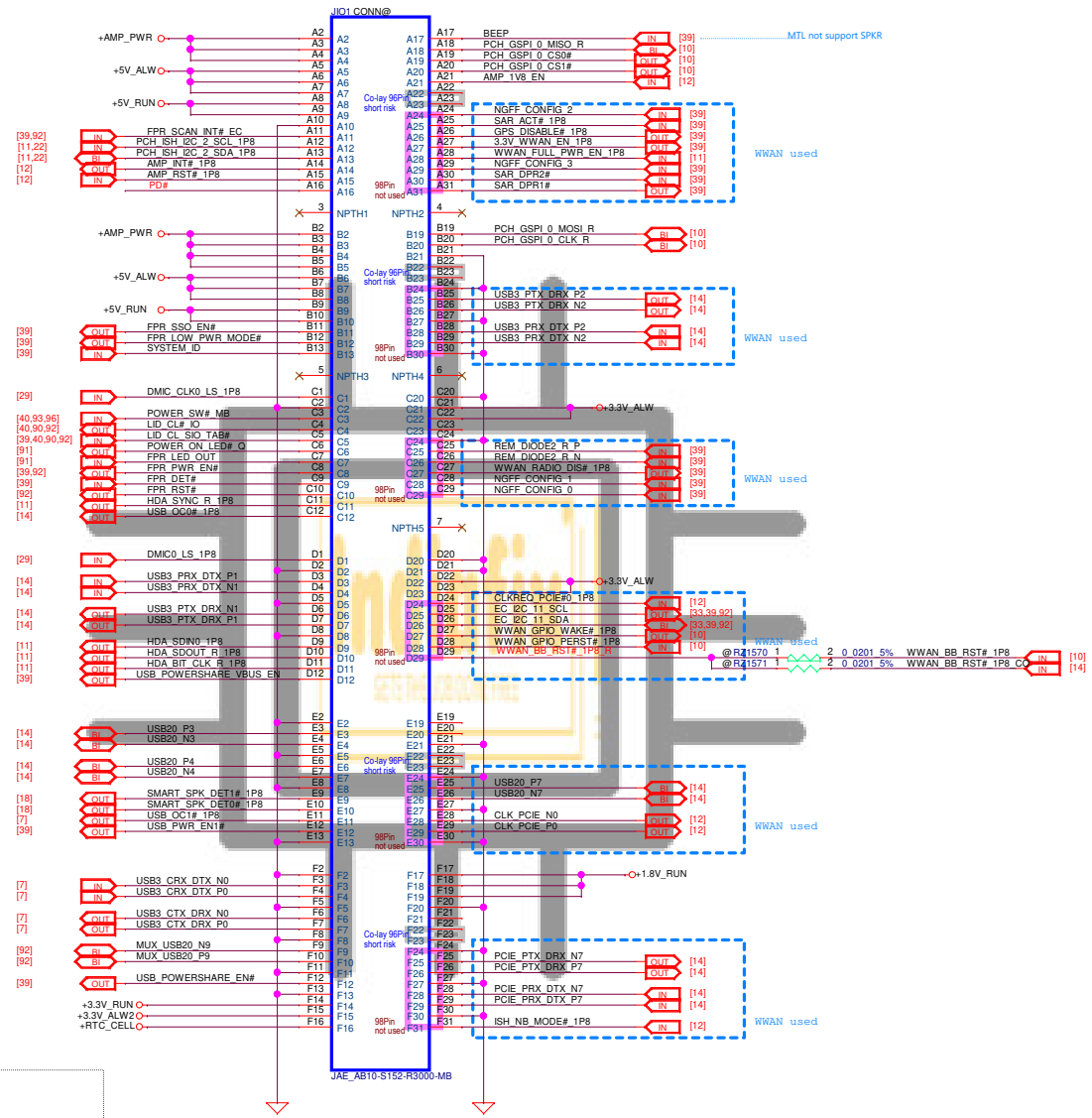
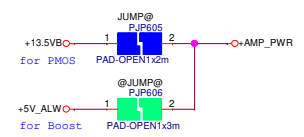
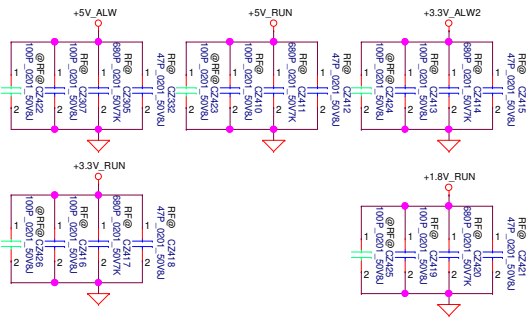


TS3A27518ERTWR						
EN#	IN1	IN2	NC1/2/3-COM1/2/3	NC4/5/6-COM4/5/6	NO1/2/3-COM1/2/3	NO4/5/6-COM4/5/6
H	X	X	OFF	OFF	OFF	OFF
L	L	L	ON	ON	OFF	OFF
L	H	L	OFF	ON	ON	OFF
L	L	H	ON	OFF	OFF	ON
L	H	H	OFF	OFF	ON	ON

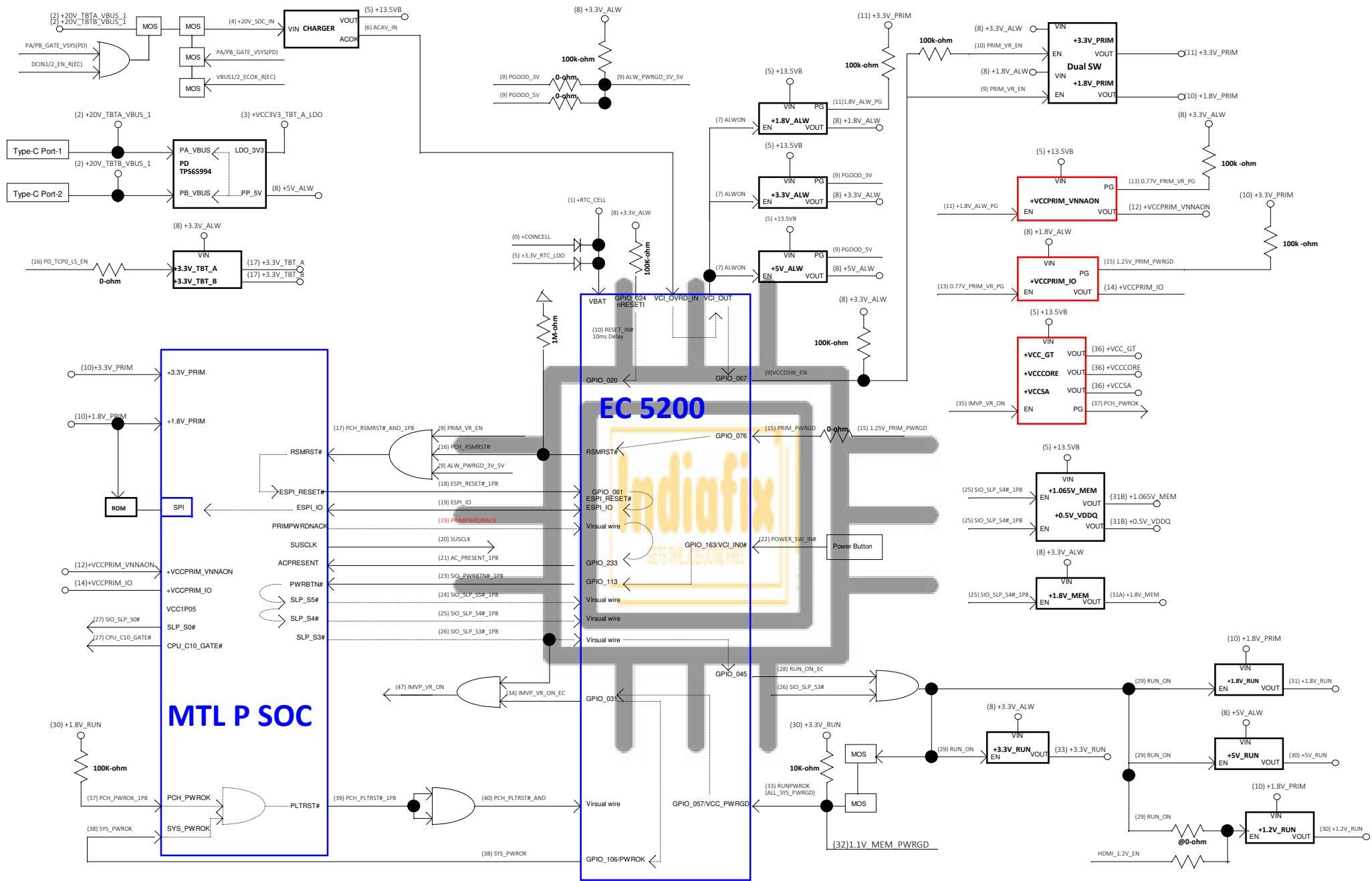
TS5A23157RSER		
IN	NC-COM	NO-COM
L	ON	OFF
H	OFF	ON

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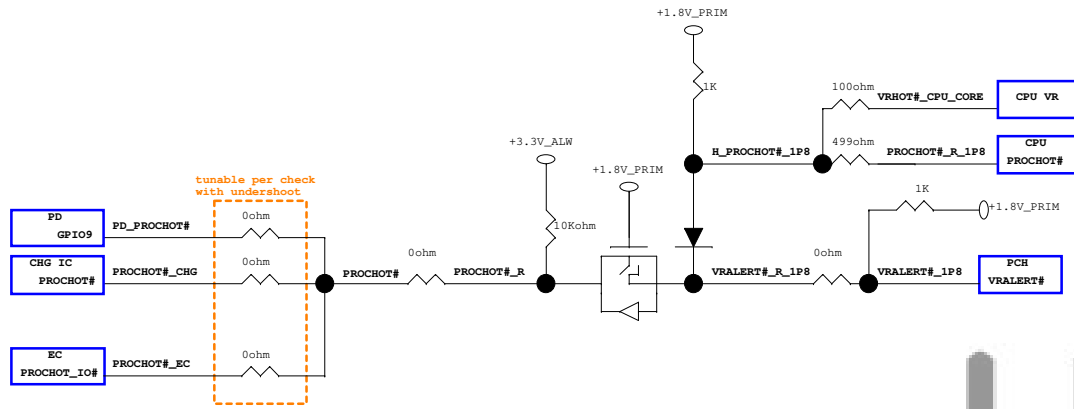
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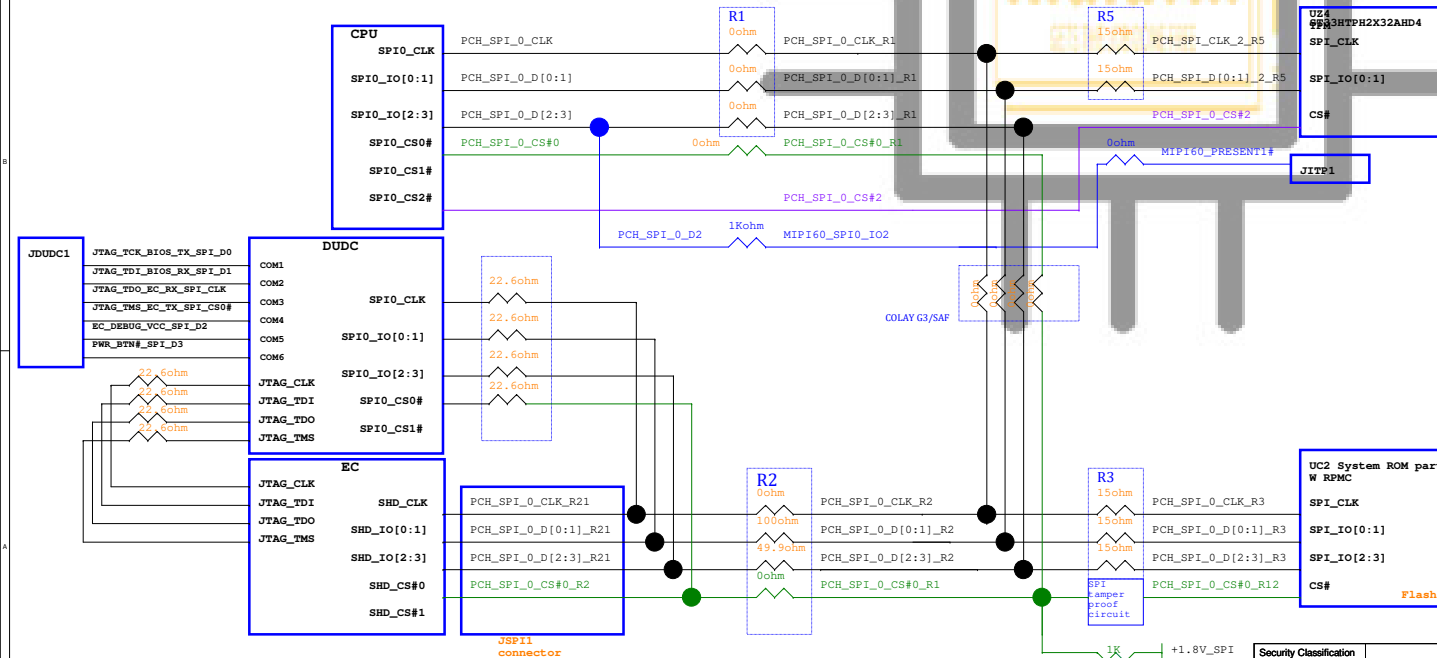
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PROCHOT# Topology



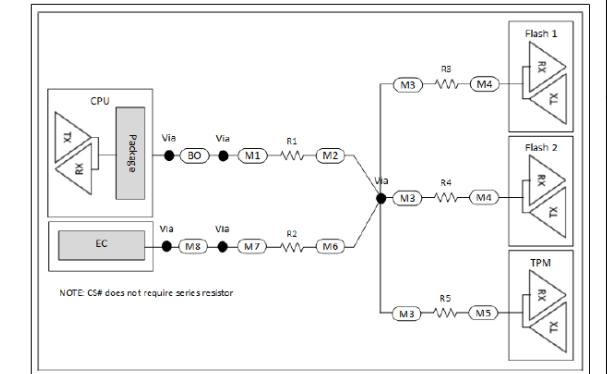
CO-LAY G3/SAF mode with Wire-OR Topology



Note	Detail
Number of vias allowed	5
Reference plane	Continuous ground only.
Max frequency	Flash 1 & Flash 2: 50 MHz. TPM: 33 MHz.
EC and CPU branch requirement	Delta between M1 + M2 and M6 + M7 shall not exceed 25.4 mm.
R1	[1] DATA: 0 Ω placeholder. To be placed on SPI0_MISO, SPI0_MOSI, SPI0_IO2 and SPI0_IO3. [2] CLK: 5 $\Omega \pm 10\%$. To be placed on SPI0_CLK.
R2	68 $\Omega \pm 5\%$. To be placed on SPI0_CLK, SPI0_MISO, SPI0_MOSI, SPI0_IO2 and SPI0_IO3.
R3	[1] 15 $\Omega \pm 10\%$. To be placed on SPI0_CLK. [2] 22 $\Omega \pm 10\%$. To be placed on SPI0_MISO, SPI0_MOSI, SPI0_IO2 and SPI0_IO3.
R4	[1] 15 $\Omega \pm 10\%$. To be placed on SPI0_CLK.

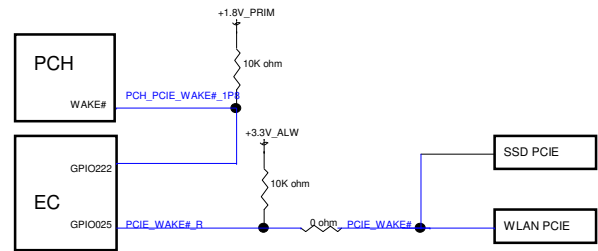
Note	Detail
R5	[2] 22 $\Omega \pm 10\%$. To be placed on SPI0_MISO, SPI0_MOSI, SPI0_IO2 and SPI0_IO3.
Minimum length	M1 and M7: 12.7 mm. BO, M2, M3, M4, M5, M6 and M8: 2.54 mm.
M3 + M4 length matching requirement	M3 + M4 segments from both branches need to be length matched within 2.54 mm.
Flash device electrical characteristics recommendation: Option 1	[1] Driver strength spec: 40 Ω or stronger across worse case corners. [2] 0.4 ns \leq rise/ fall time measured at 30% to 70% ≤ 1.25 ns based on 30 pF test load. [3] Output capacitance, Cout ≤ 14 pF (including RPMC die). [4] Input capacitance, Cin ≤ 12 pF (including RPMC die). [5] Data input setup time ≤ 3 ns. [6] Data input hold time ≤ 3 ns. [7] CLK to DATA output valid time, min: 1 ns, based on 30 pF test load. [8] CLK to DATA output valid time, max: 9 ns (50% to 50%), based on 30 pF test load.
Flash device electrical characteristics recommendation: Option 2	[1] Driver strength spec: 50 Ω or stronger across worse case corners. [2] 0.4 ns \leq rise/ fall time measured at 30% to 70% ≤ 1.45 ns based on 30 pF test load. [3] Output capacitance, Cout ≤ 16 pF (including RPMC die). [4] Input capacitance, Cin ≤ 12 pF (including RPMC die). [5] Data input setup time ≤ 3 ns. [6] Data input hold time ≤ 3 ns. [7] CLK to DATA output valid time, min: 1 ns, based on 30 pF test load. [8] CLK to DATA output valid time, max: 6.5 ns (50% to 50%), based on 30 pF test load.
Length matching between CLK and DATA/ CS# signals	12.7 mm
Trace spacing between DATA and DATA signals	0.250 mm
Trace spacing between CLK and DATA/ other signals	0.375 mm
Signal name/ list	SPI0_CLK, SPI0_MOSI, SPI0_MISO, SPI0_IO2, SPI0_IO3, SPI0_CS[0:1]# (for Flash), SPI0_CS2# (for TPM).

Figure 274. SPI0 3-Load Branch (Device Down) with EC Wired-OR Flash Sharing Topology Diagram

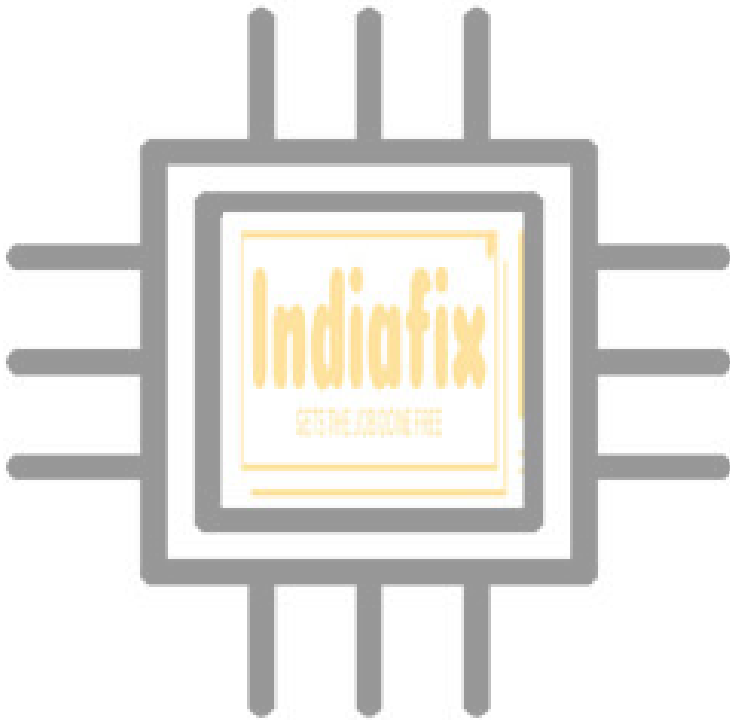
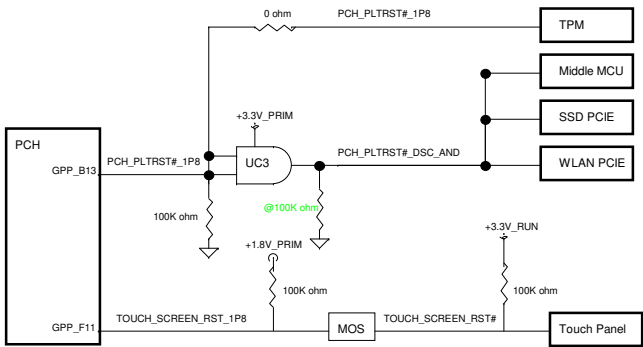


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PCH_PCIE_WAKE# Topology

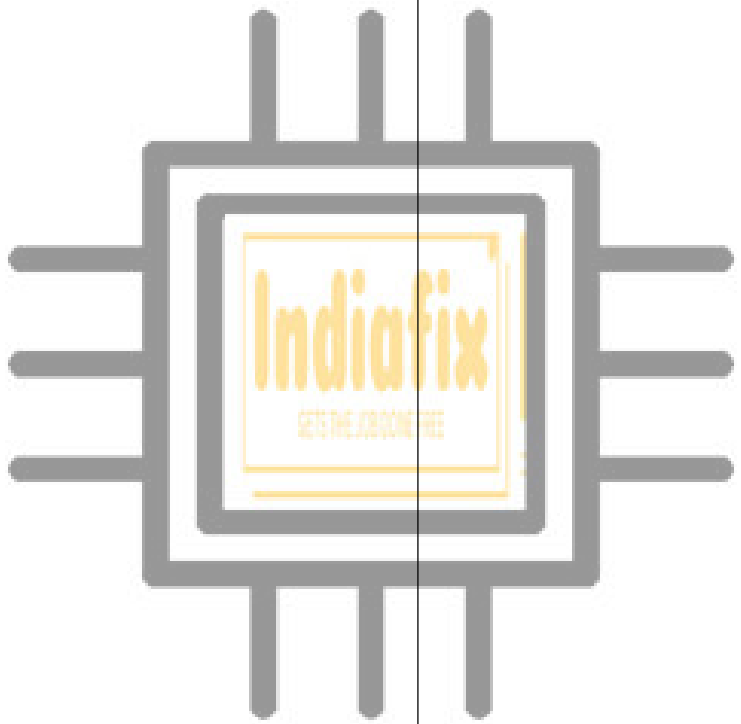


PCH_PLTRST# Topology



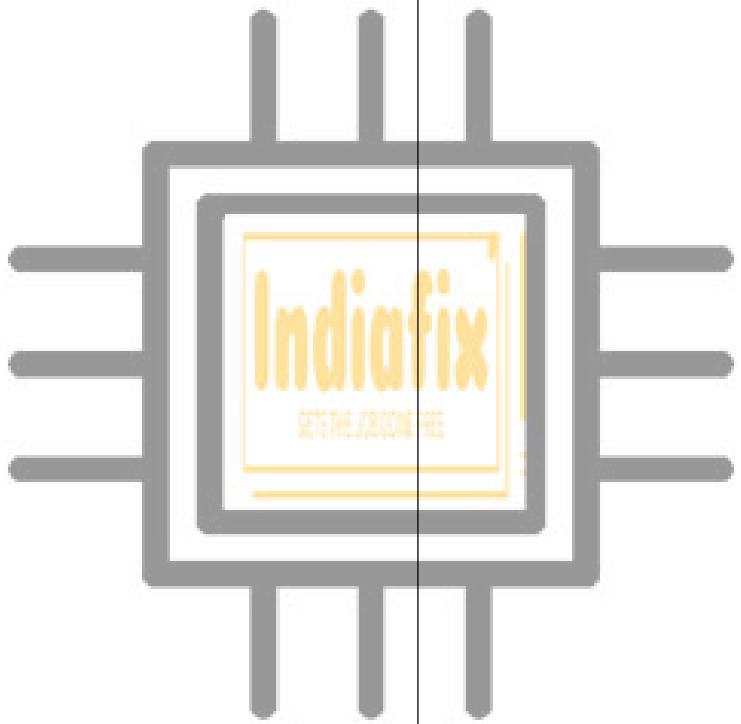
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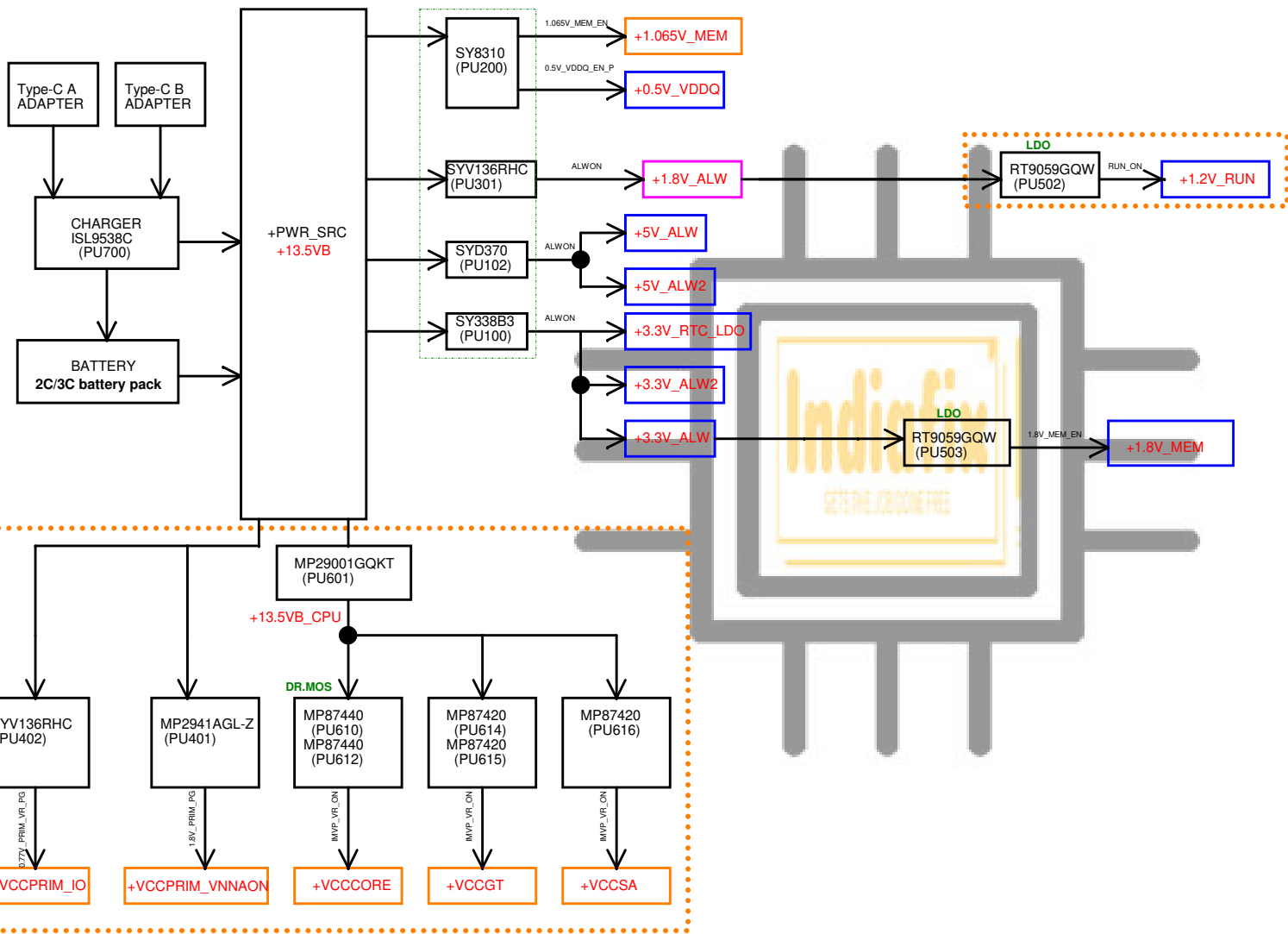
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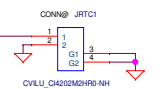
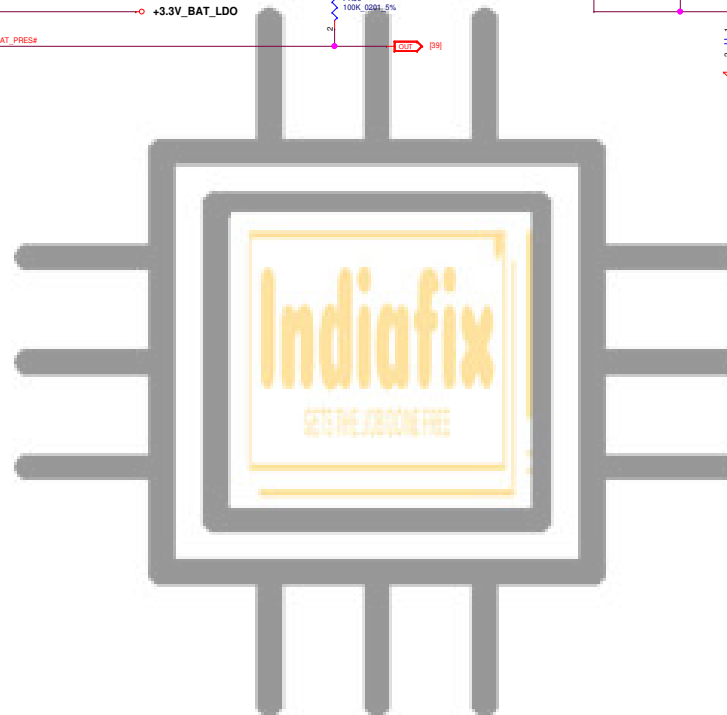
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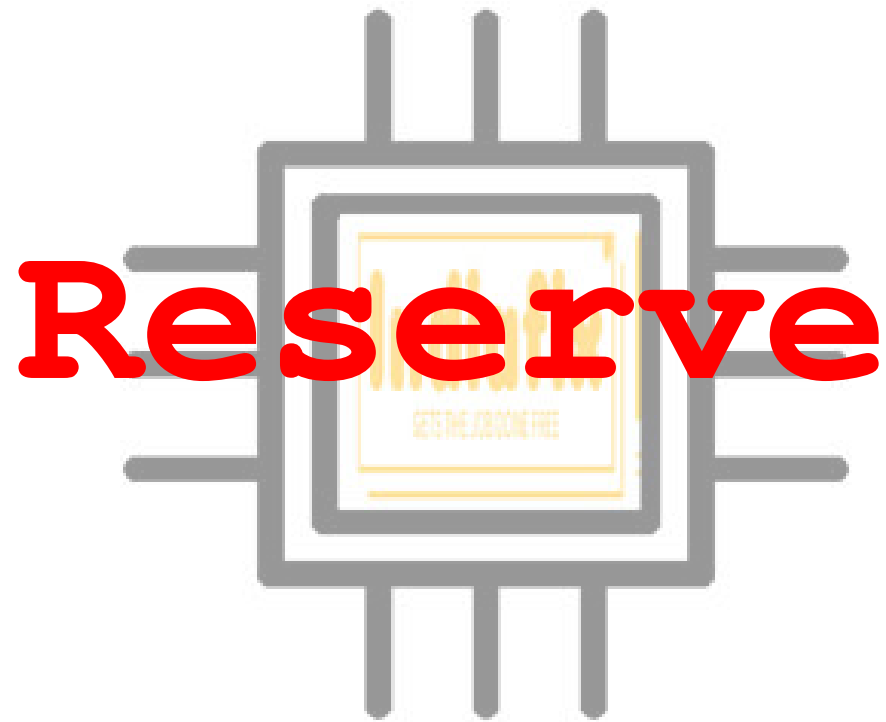
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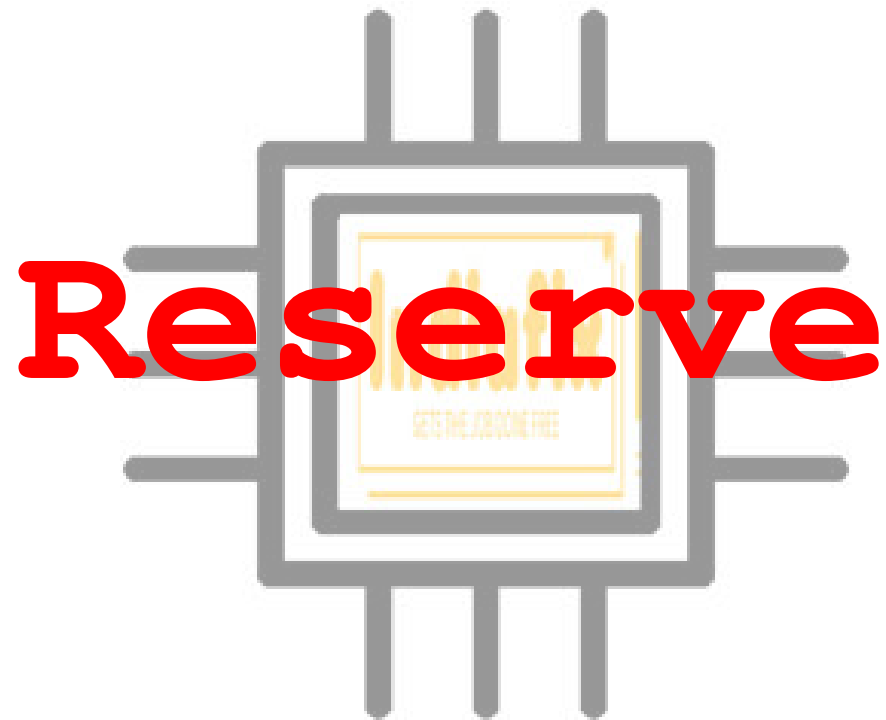


CPU PWR
PCH PWR
Peripheral Device PWR





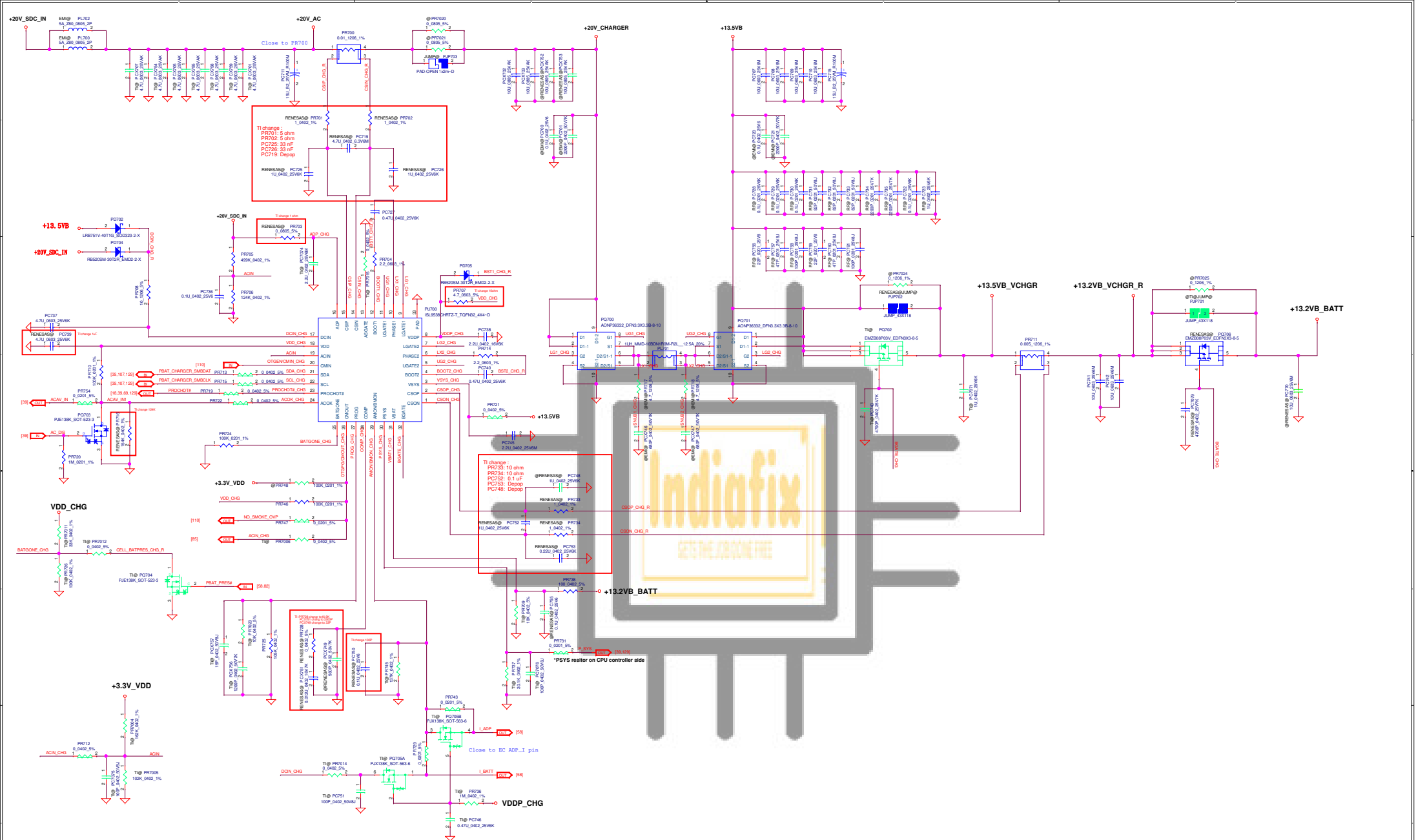
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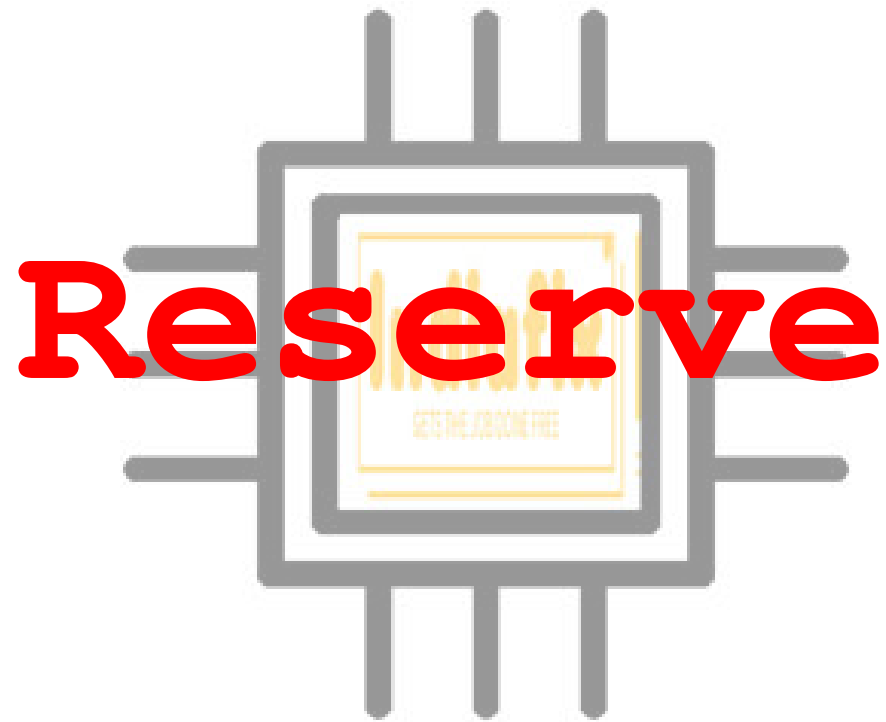
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Reserve

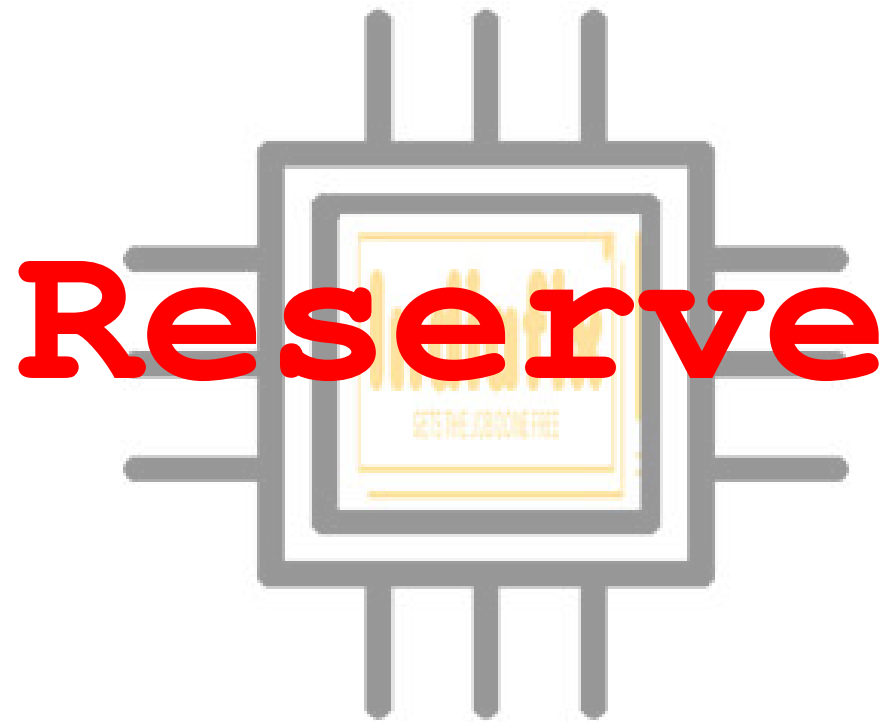
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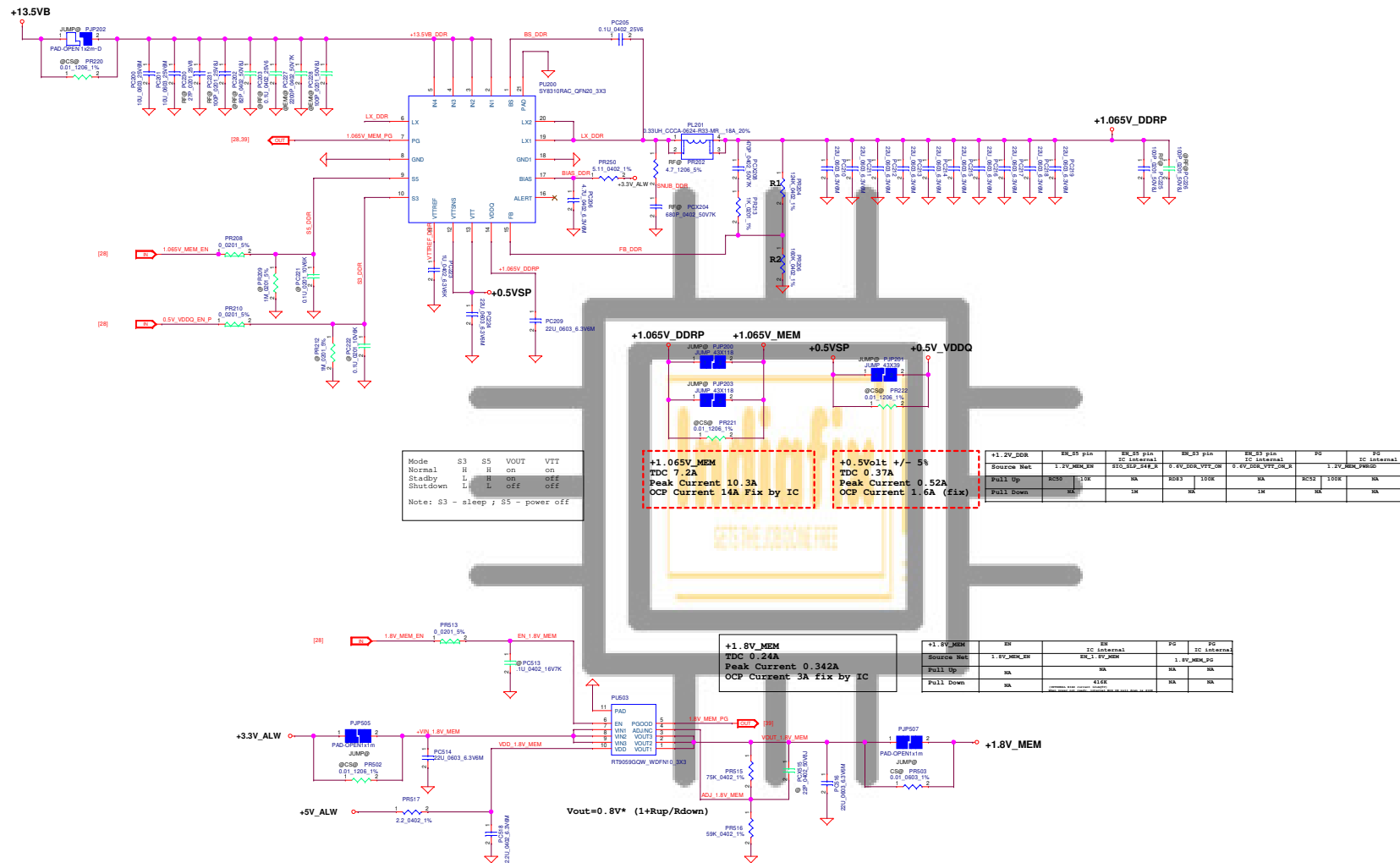
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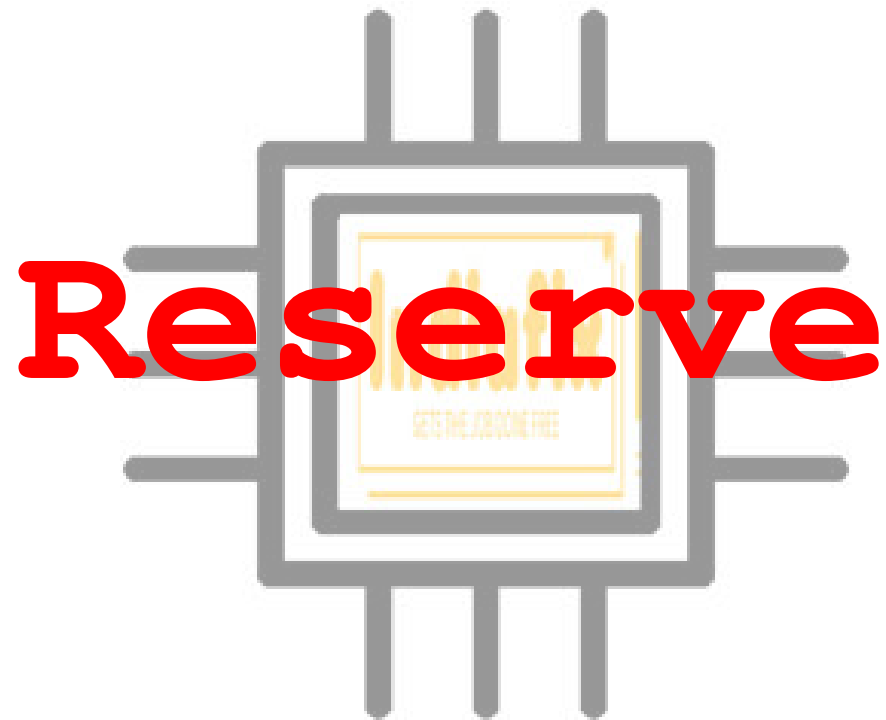


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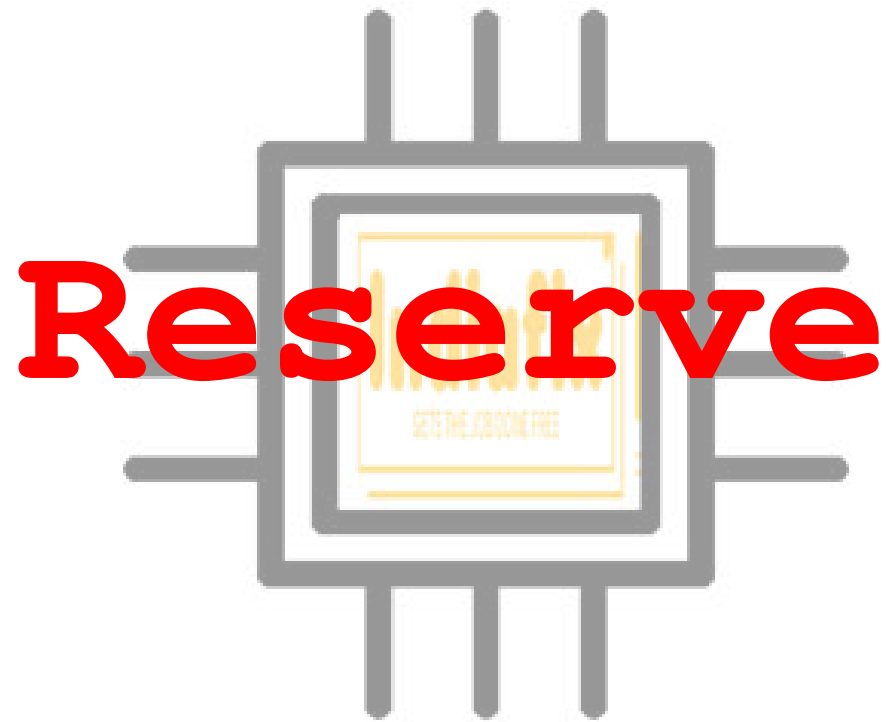


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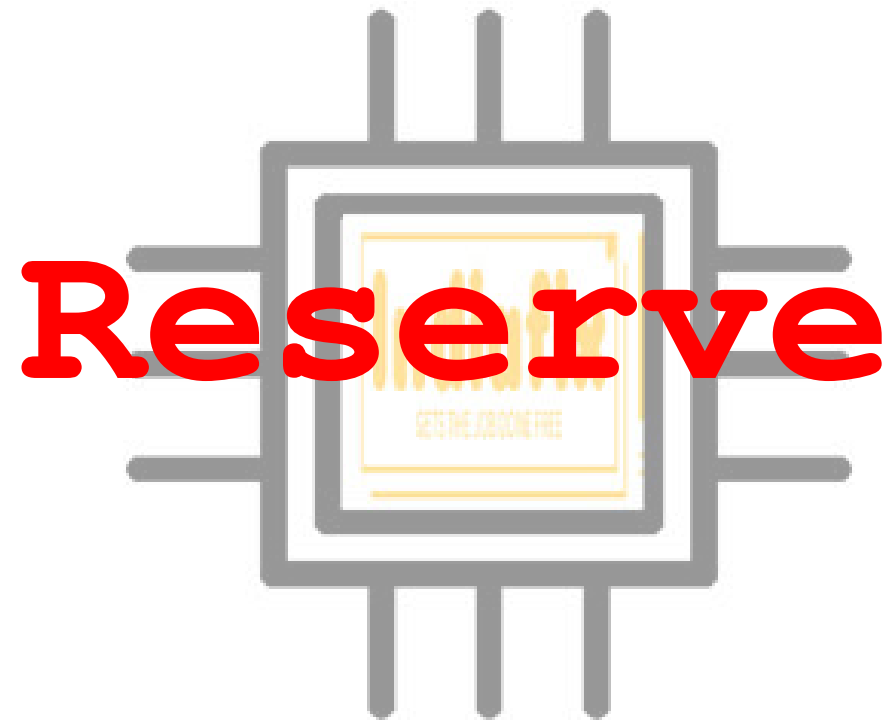




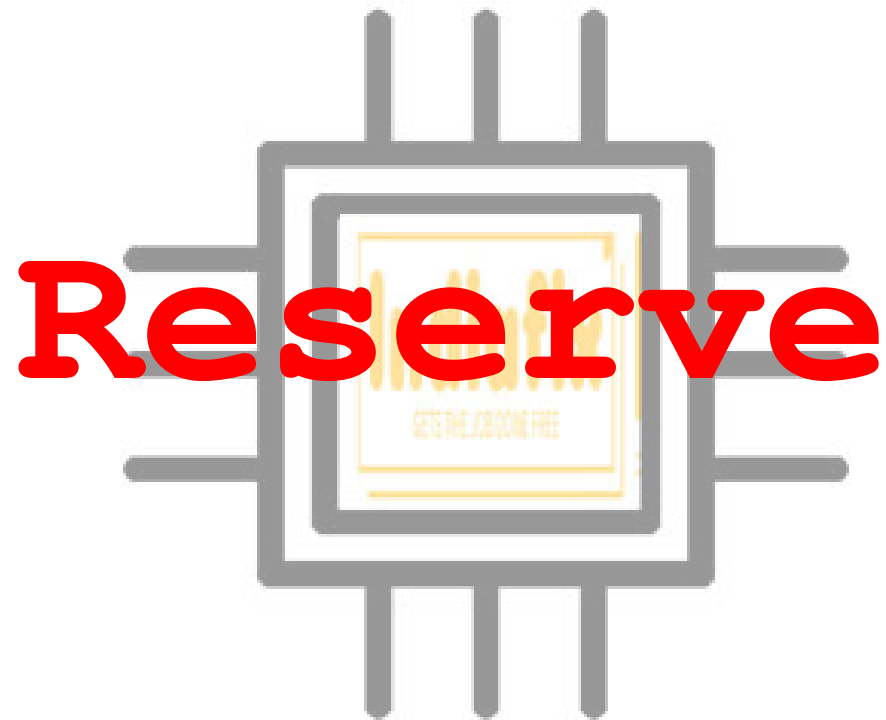
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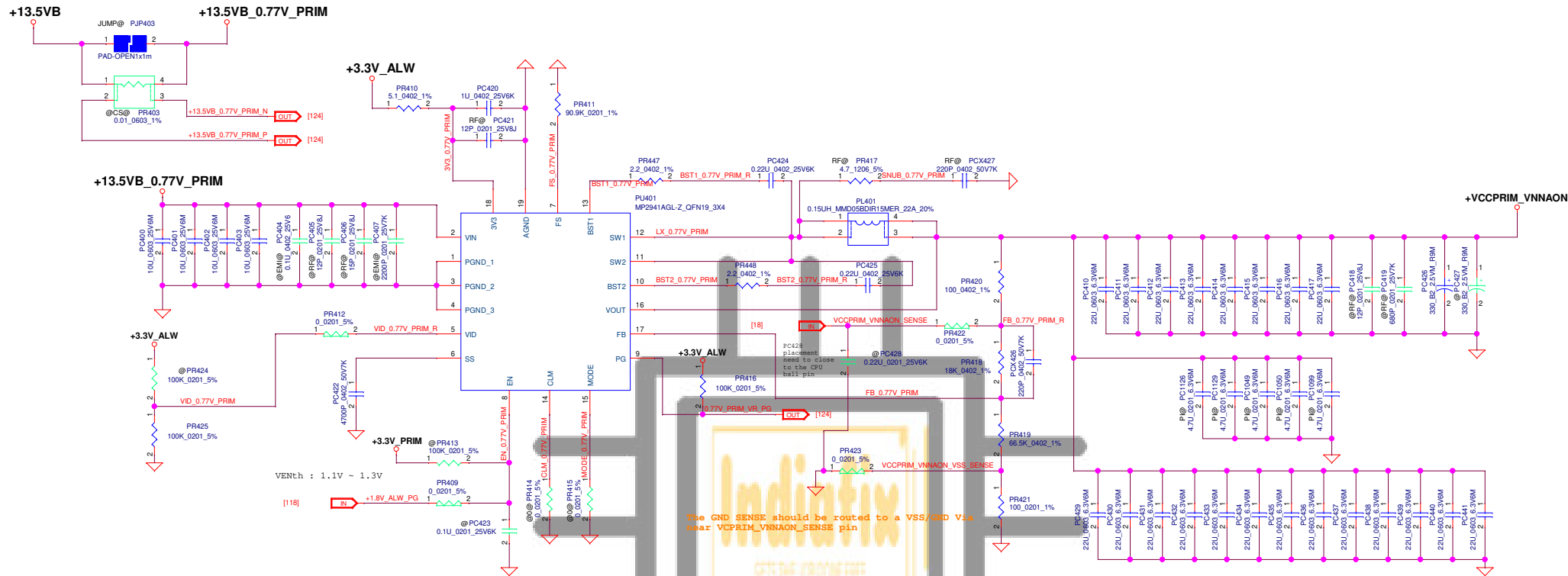
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The GND SENSE should be routed to a VSS/GND VSS near VCCPRIM_VNNAON_SENSE pin

$V_{FB} = 0.6V$
 $V_{out} = 0.6V * (1 + R1/R2)$
 $V_{out} = 0.77V$

Table---1:VID control Bit logics

VID	Reference (V)	Reference (V)	Reference (V)
	min	typ	max
0		0.6	
1	1.182	1.2	1.218

Table---2:CLM Select

State	CLM	Resistor to GND
M1	7A	0
M2	10A	90k
M3	13A	150k
M4	17A	>230k or float

Table---3:MODE Select

State	Interleaving	VID Down option	Resistor to GND
M1	N	Slew down	0
M2	Y	Slew down	90k
M3	Y	Decay	150k
M4	N	Decay	>230k or float

Table---4:FS Select

State	f _s (kHz)	Resistor to GND
M1	500	0
M2	100	90k
M3	1000	150k
M4	1200	>230k or float

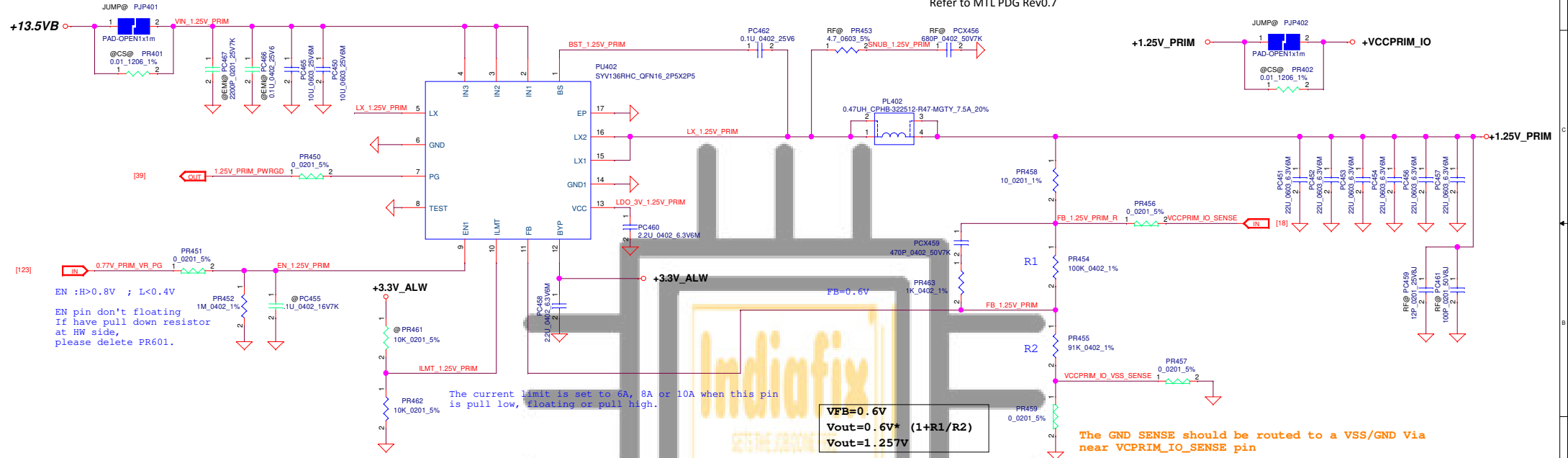
+VCCPRIM_VNNAON (MTL-U 15W_Performance)
 Peak Current 17.68A (ICCmax)
 TDC : 8.84A
 DC Load line : NA
 AC Load line : NA
 Current limit : 34A(min) by IC pin.14 setting
 Fsw=700kHz

+VCCPRIM_VNNAON (MTL-H 28W_Baseline)
 Peak Current 19.95A (ICCmax)
 TDC : 9.97A
 DC Load line : NA
 AC Load line : NA
 Current limit : 34A(min) by IC pin.14 setting
 Fsw=700kHz

+VCCPRIM_VNNAON	EN	EN	PG	PG
Source Net	+1.8V_ALW_PG	IC Internal	0.77V_PRIM_VR_PG	IC Internal
Pull Up	PR313 100k	NA	PR416 100k	NA
Pull Down	NA	1.2M	NA	NA

+VCCPRIM_IO (MTL-P 28W)
TDC 0.91A
ICCMAX 1.3A
Itrip NA
OCF 6A
Fsw=500kHz

Refer to MTL PDG Rev0.7



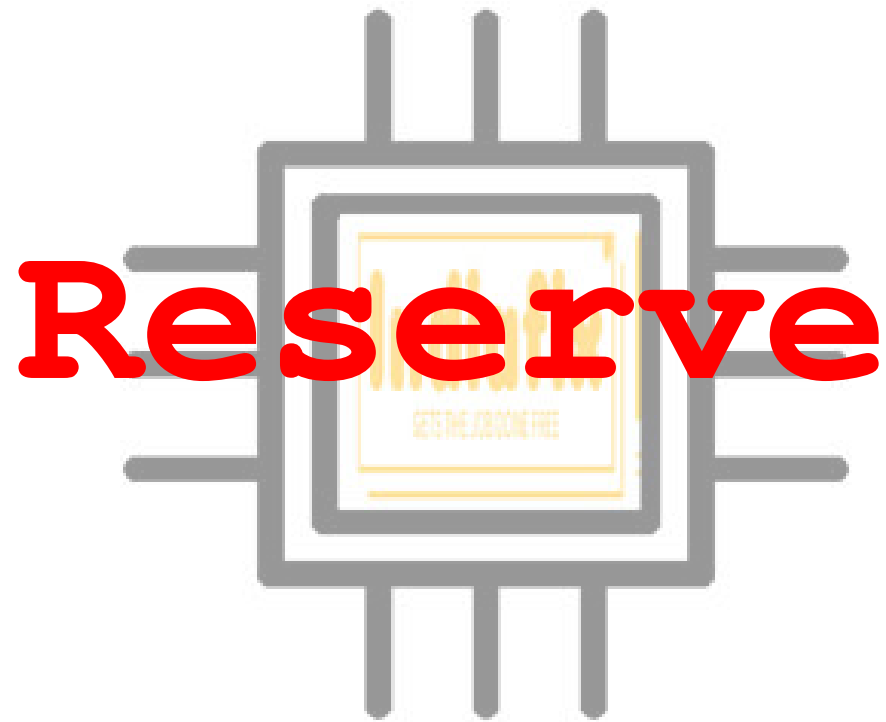
+VCCPRIM_IO	EN	IC internal	PG	PG
Source Net	0.77V_PRIM_VR_PG	EN_1_25V_PRIM	1.25V_PRIM_PWRGD	IC internal
Pull Up	NA	NA	RES06 100K	NA
Pull Down	PR452 1M	2.5M	NA	NA

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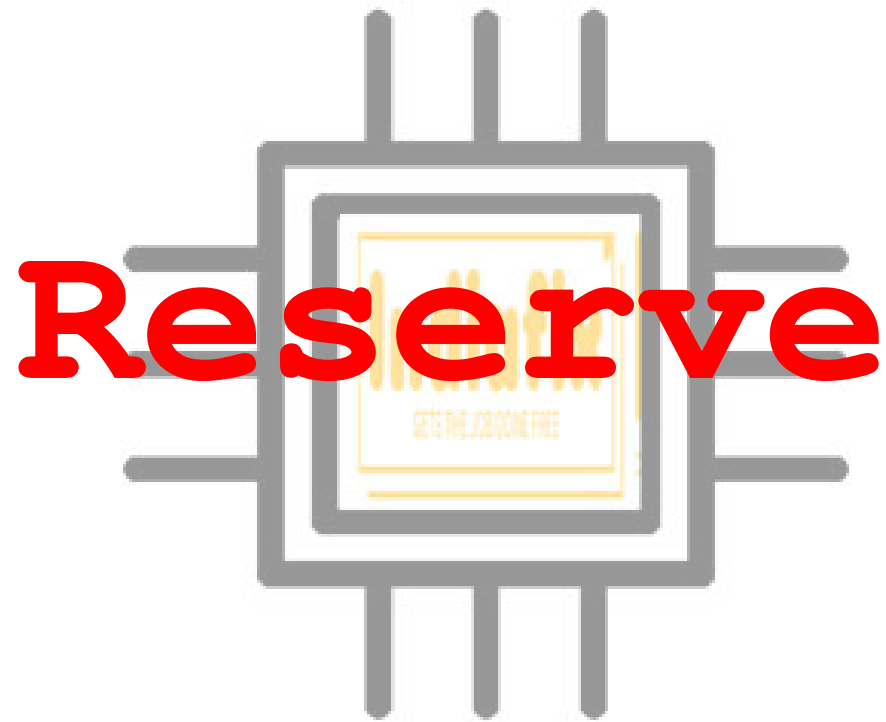
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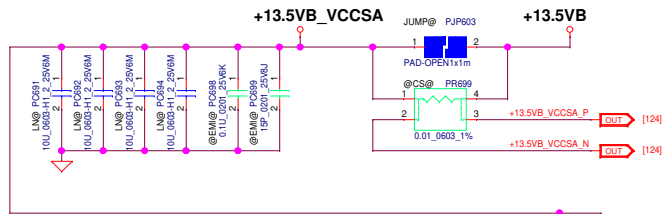
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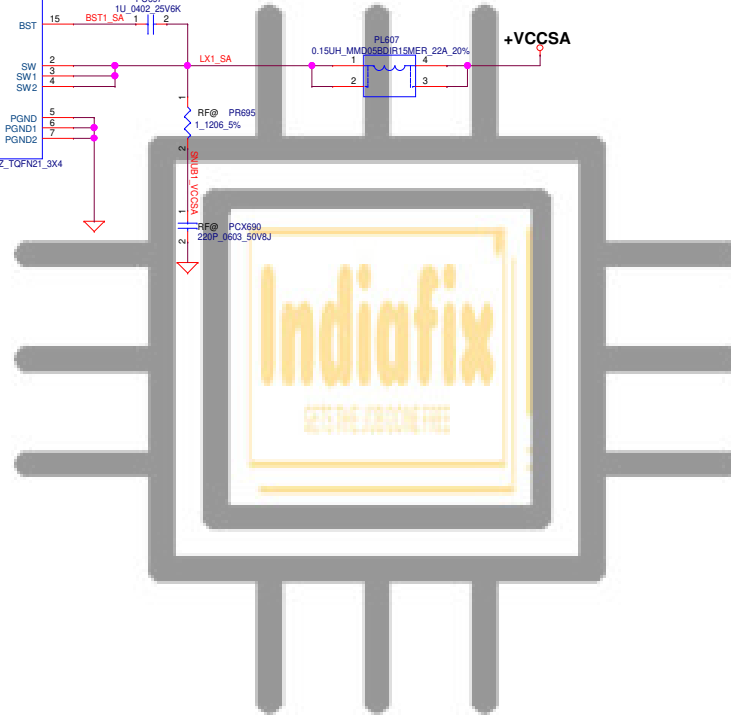
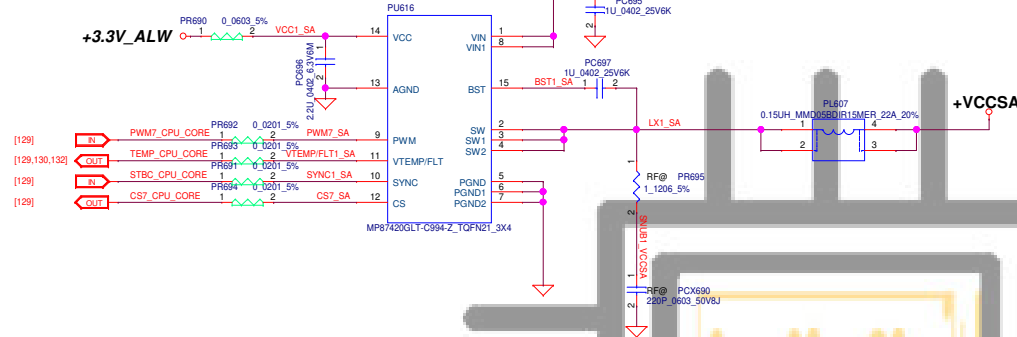
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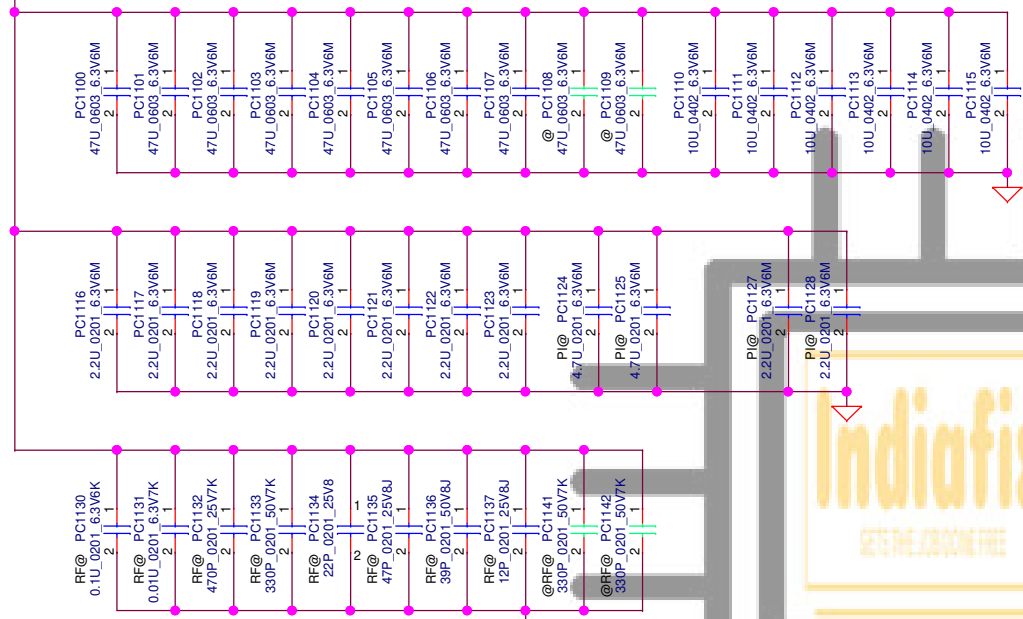


+VCCSA (MTL-U 15W_Performance/MTL-H 28W_Baseline)
ICCMAX = 35 A
ITRIP = 27 A
TDC = 15 A
OCF = 45.5 A
DC LL = 4.9 mohm
AC LL = 4.9 mohm
Fsw = 600 kHz

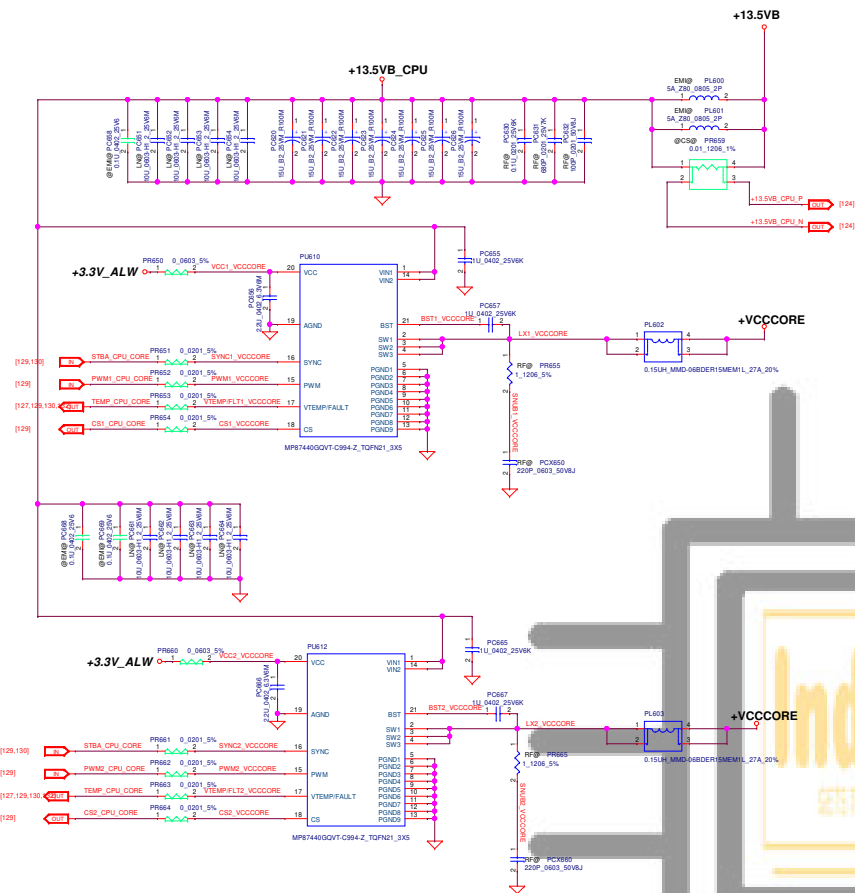


+VCCSA Decoupling
47U_0603 *8 pcs + Reserve *2 pcs
10U_0402 *6 pcs
2.2U_0201 *8 pcs

+VCCSA

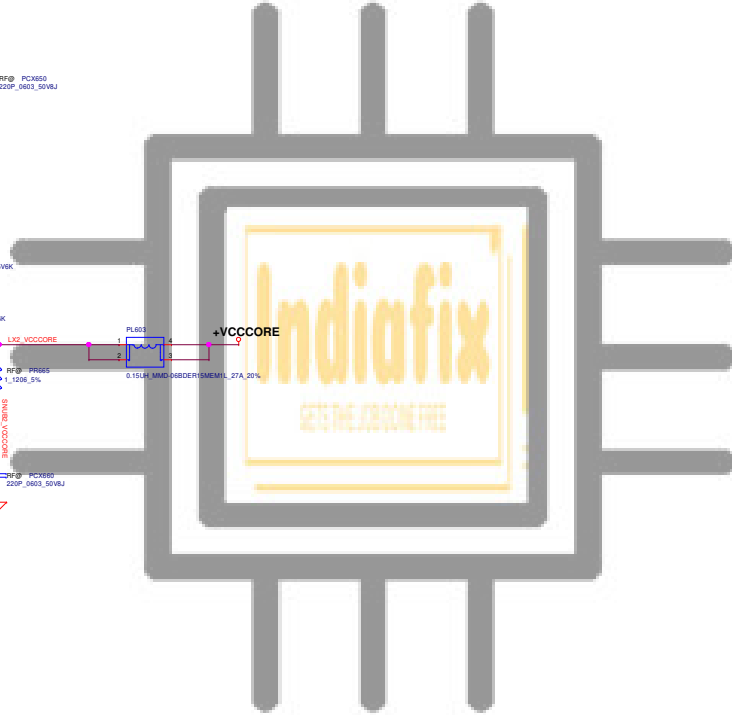


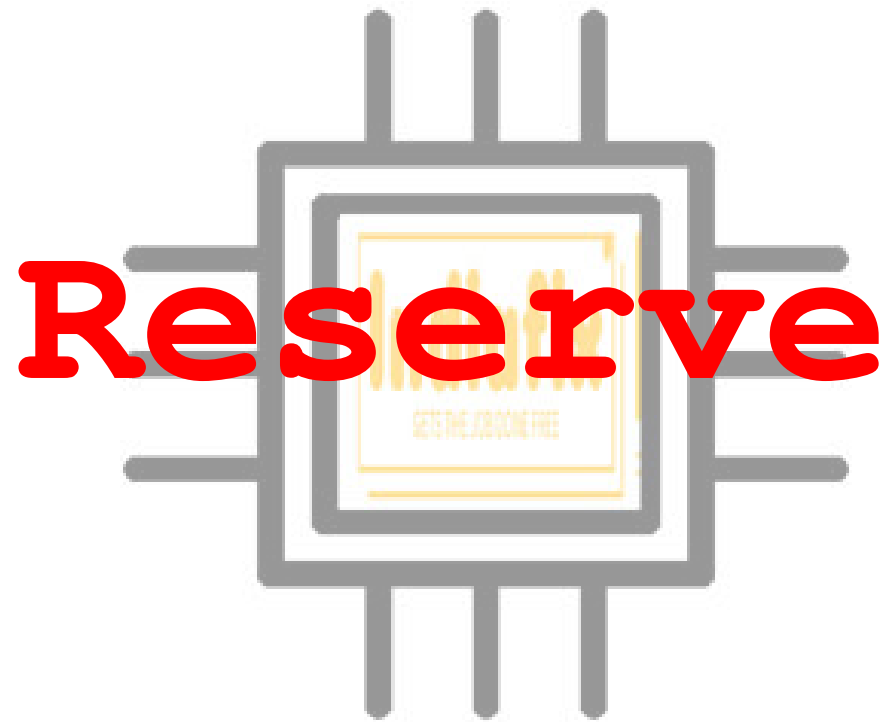
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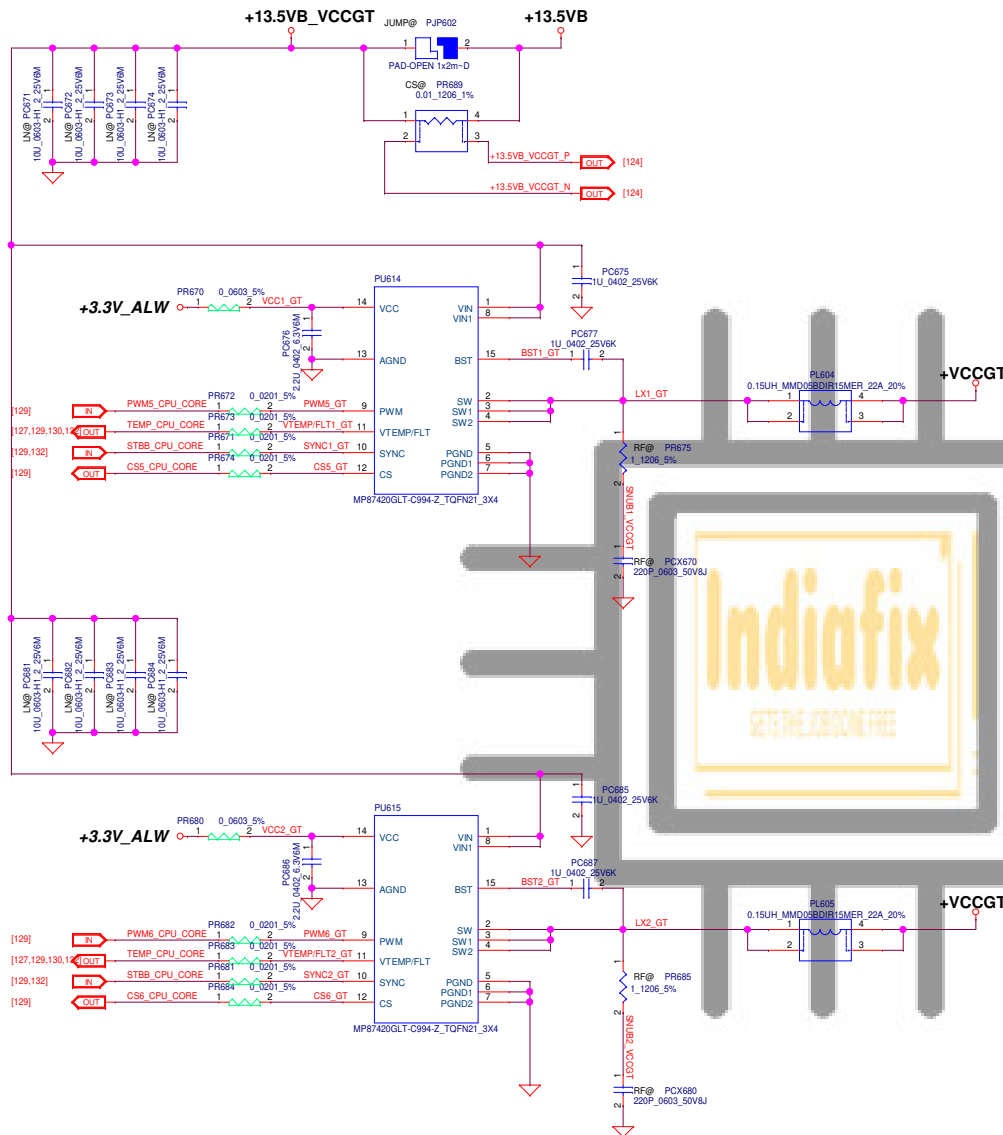
+VCCORE (MTL-U 15W_Performance)
 ICCMAX = 94 A
 ITRIP = 70 A
 TDC = 46 A
 DC LL = 1.9 mohm
 AC LL = 1.9 mohm
 Fsw = 600 kHz

+VCCORE (MTL-H 28W_Baseline)
 ICCMAX = 80 A
 ITRIP = 71 A
 TDC = 46 A
 DC LL = 1.9 mohm
 AC LL = 1.9 mohm
 Fsw = 600 kHz





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+VCCGT (MTL-U 15W_Performance)

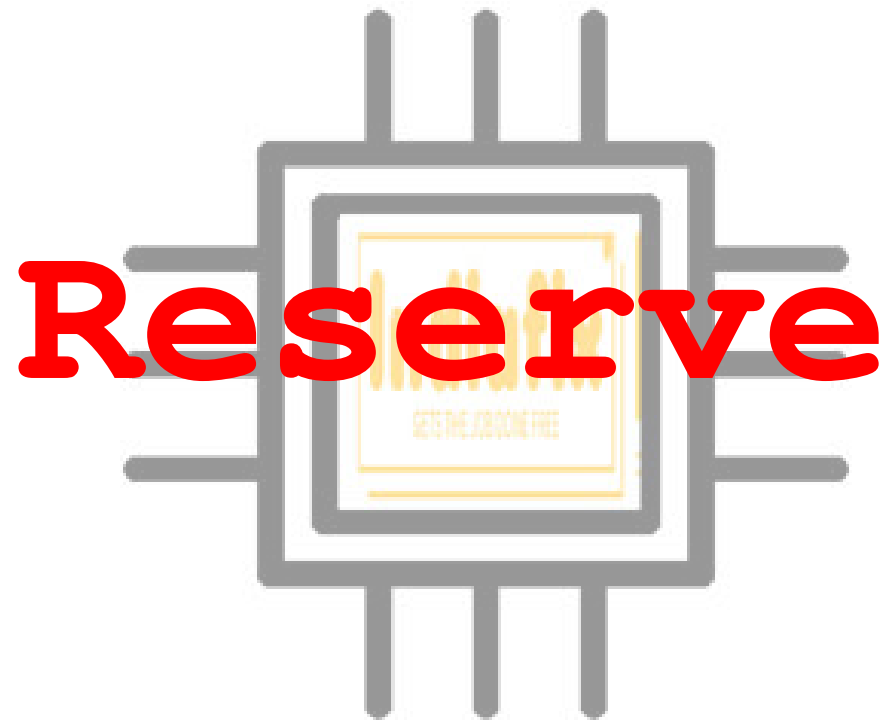
ICCMAX = 40 A
TDC = 14.3A
OCP = 49.4A
DC LL = 3.1 mohm
AC LL = 3.1 mohm
Fsw = 600 kHz

+VCCGT (MTL-H 28W_Baseline)

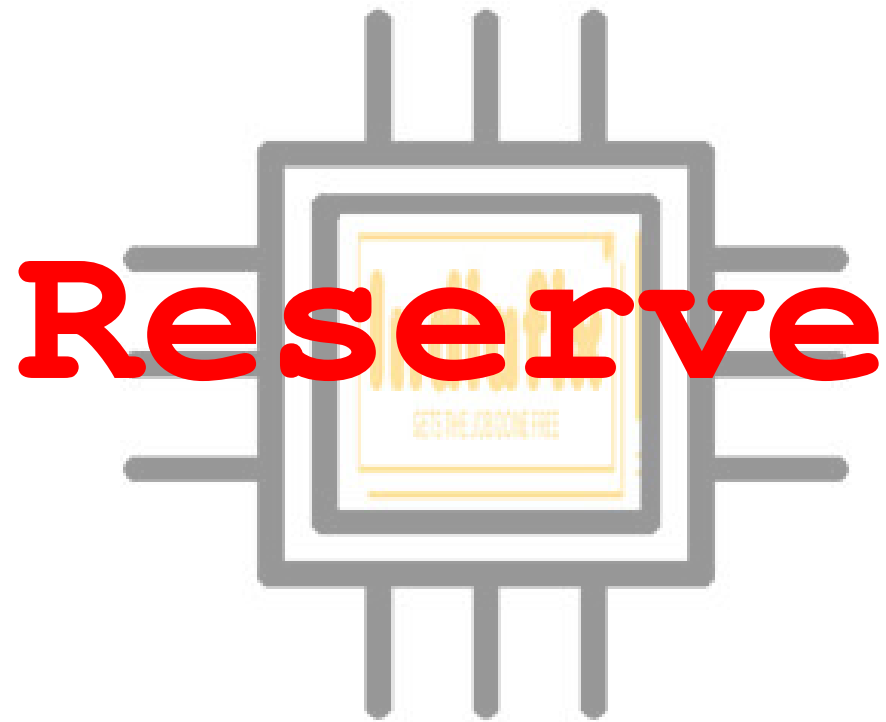
ICCMAX = 59 A
ITRIP = 43 A
TDC = 23 A
OCP = 76.7 A
DC LL = 3.1 mohm
AC LL = 3.1 mohm
Fsw = 600 kHz



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CPU Decoupling CAP					
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Date	Issued - December 1st 2020	Revised	13 of 13		50



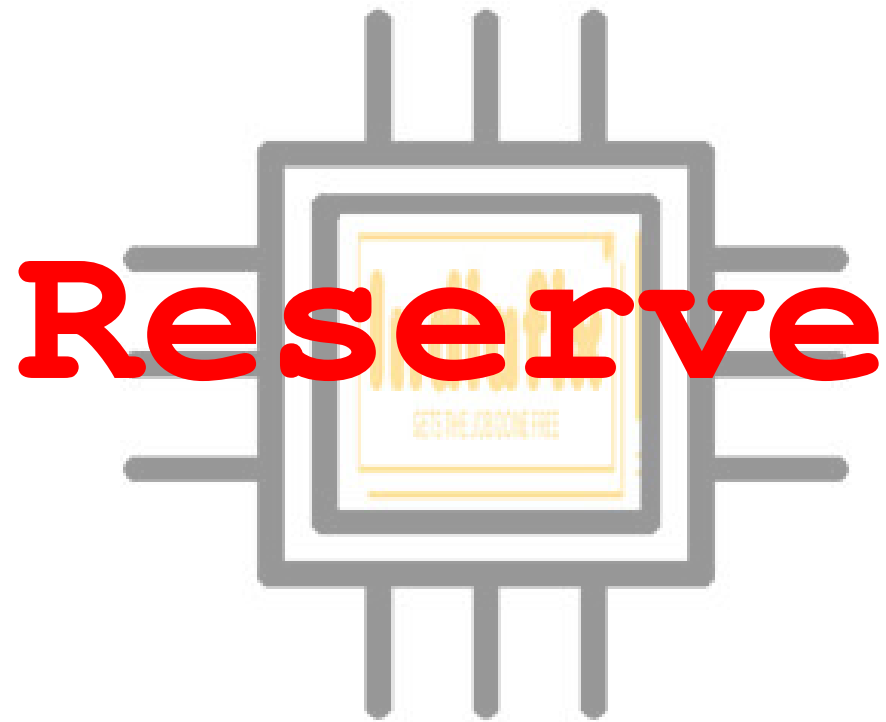
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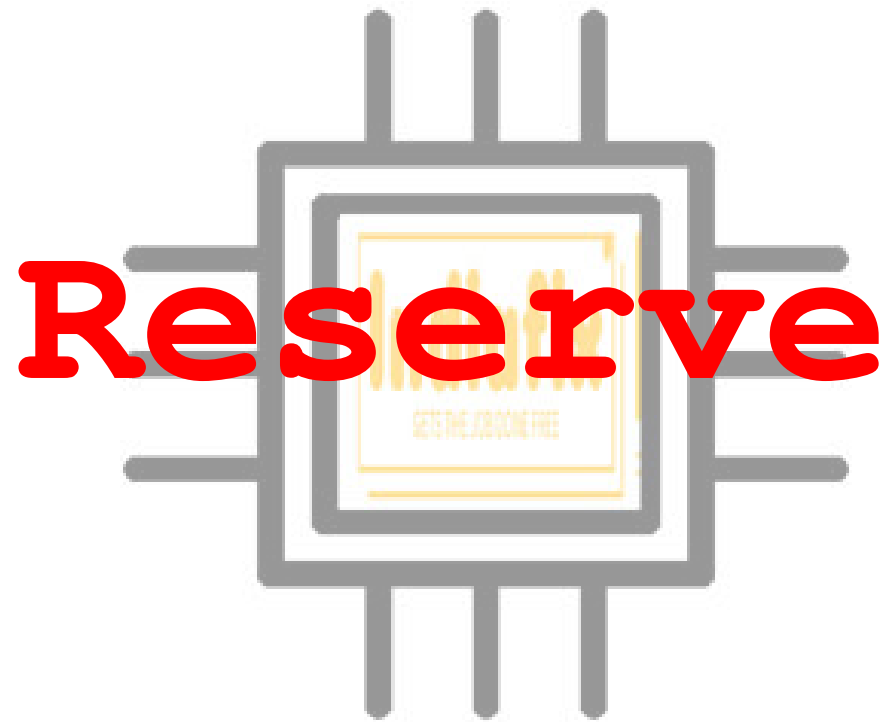
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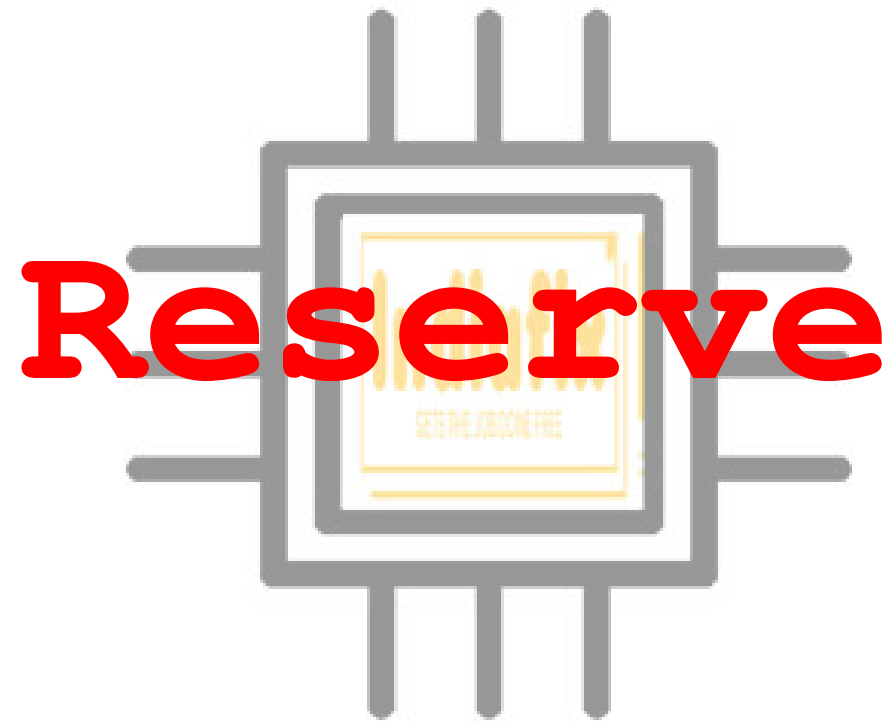
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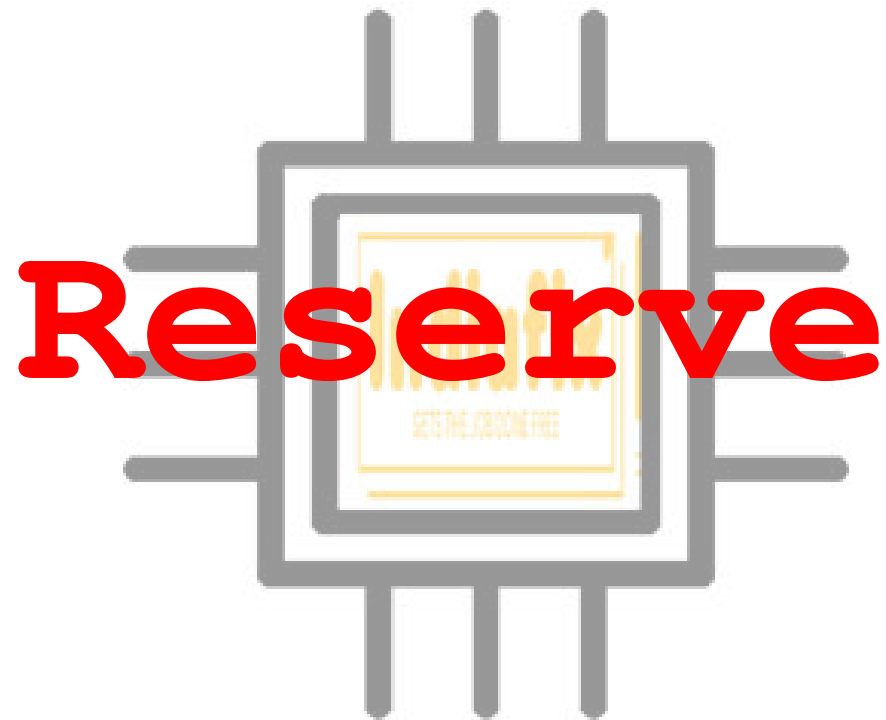
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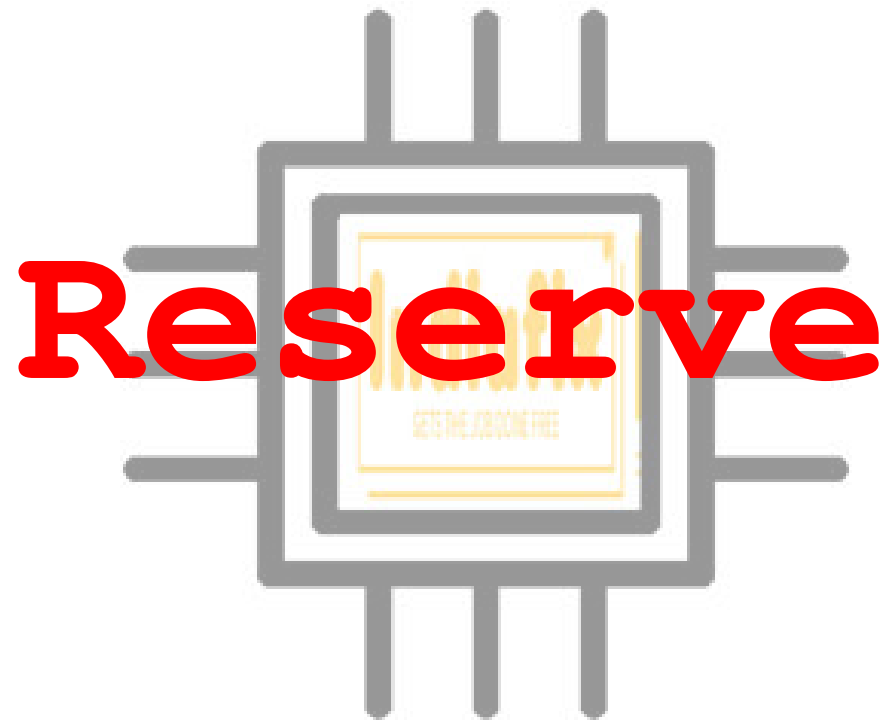
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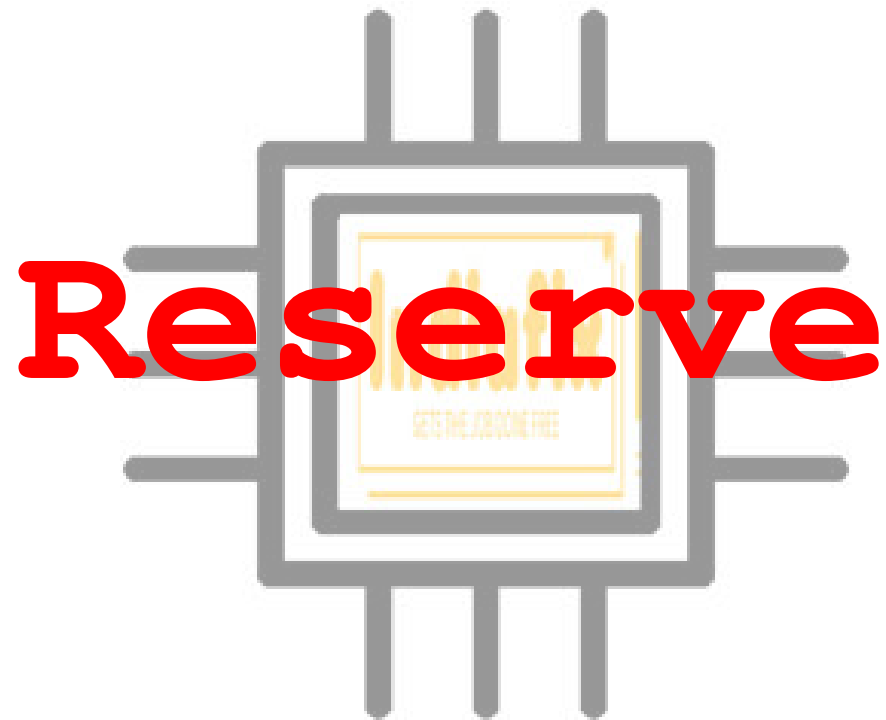
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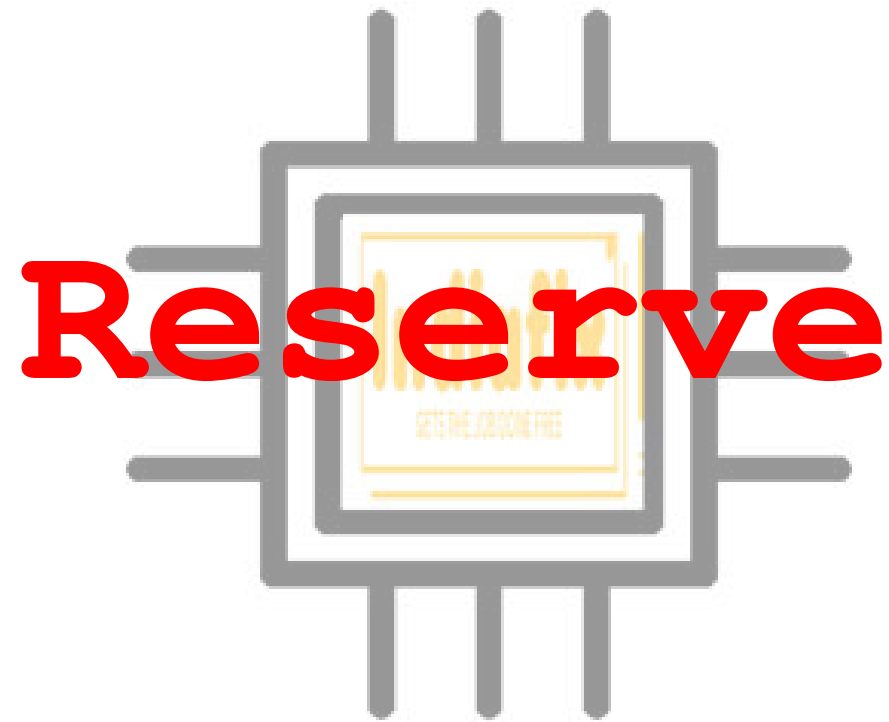
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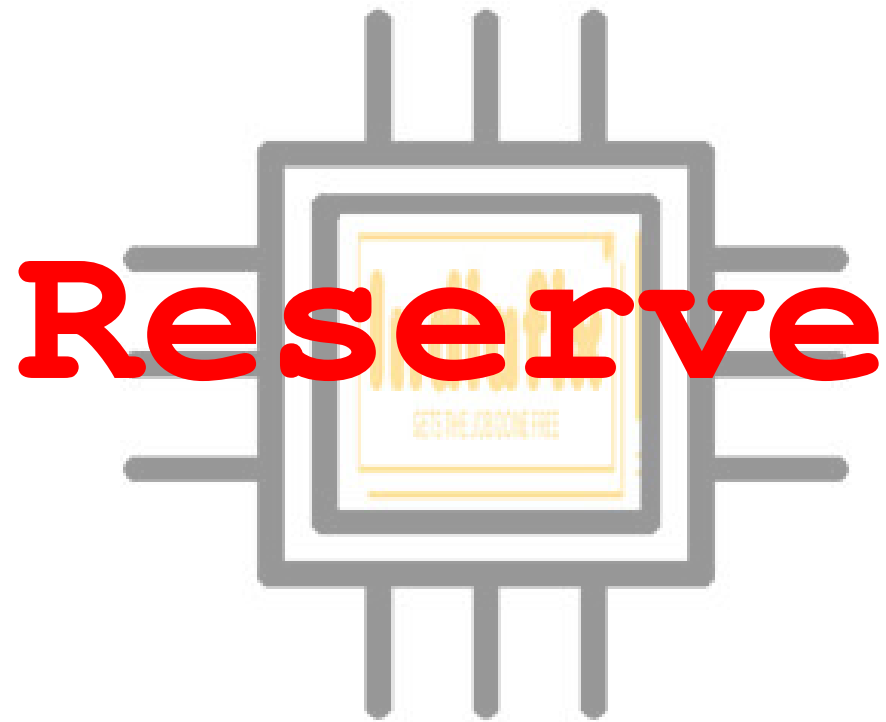


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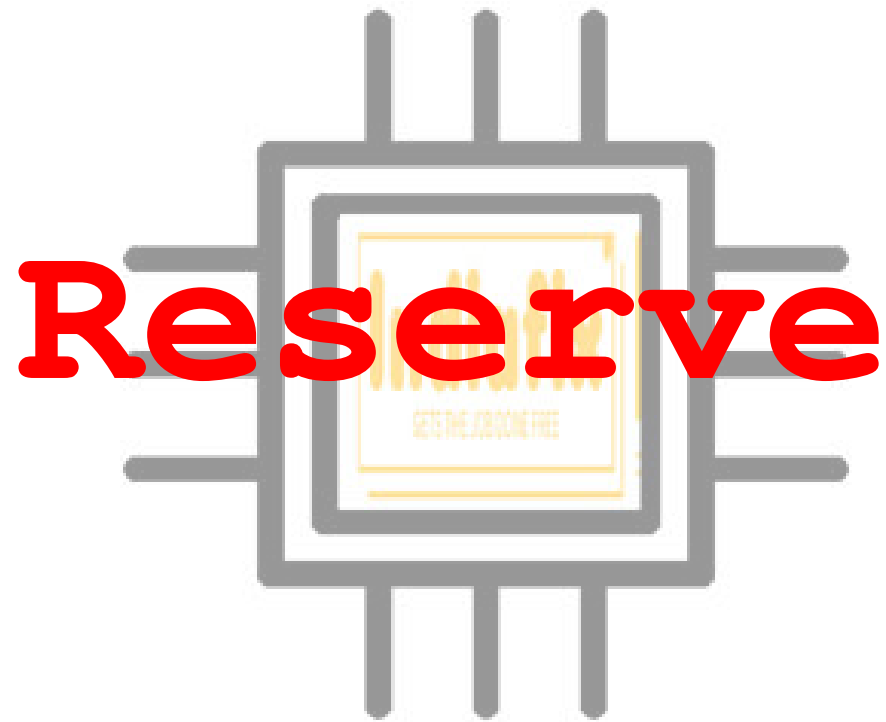


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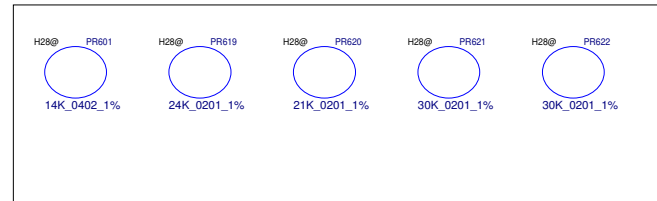


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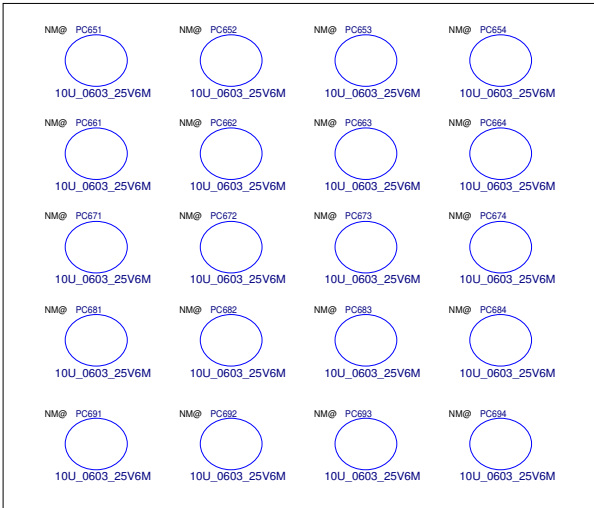
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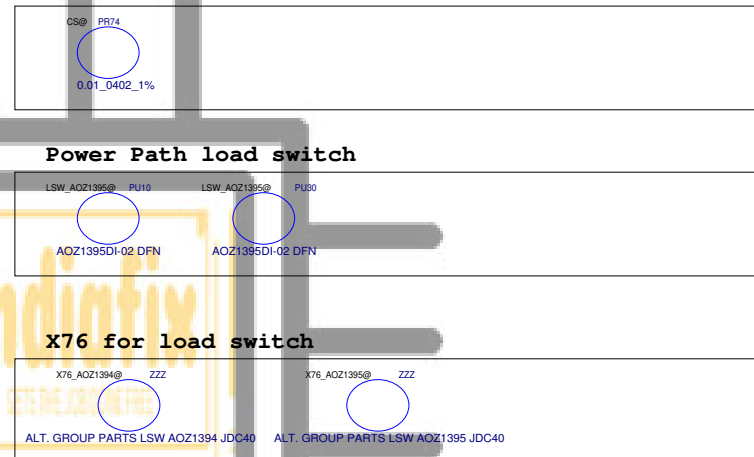


	Location	U15	MTL-U 15W	H28	MTL-H 28W
Psys	PR601	V	11.3K	V	14K
IA IMON	PR619	V	38.3K	V	24K
	PR620	V	0	V	21K
GT IMON	PR621	V	66.5K	V	30K
	PR622	V	24K	V	30K

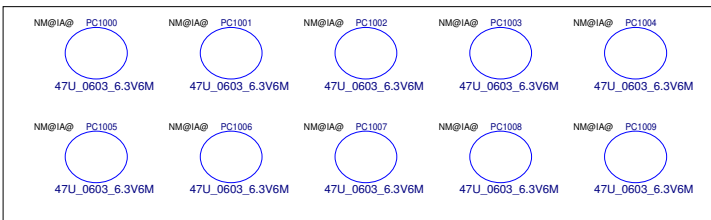
CPU Input Low noise MLCC



FIP Board



+VCC_CORE Output Low noise MLCC



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